

Development of the Triggerless DAQ System for the SPD Experiment at the NICA Collider

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Spin Physics Detector

SETUP

Stage 1:

- Duration: ~2 years
- 6 Detector subsystems + part of ECal endcap
- Interaction rate $4x10^5$
- Data rate ~1 GB/s

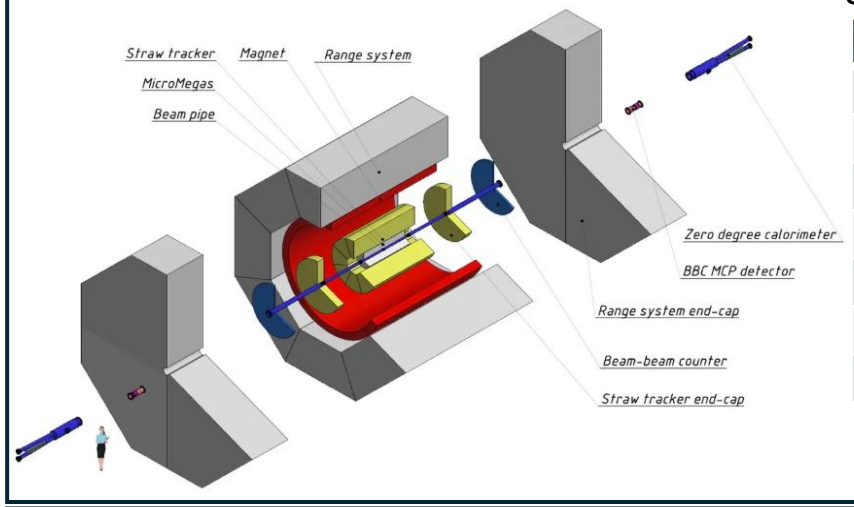
Stage 2:

- Duration: 4+ years
- 9 Detector subsystems
- Interaction rate $4x10^6$
- Data rate 20+ GB/s

Bunch crossing: 76 ns

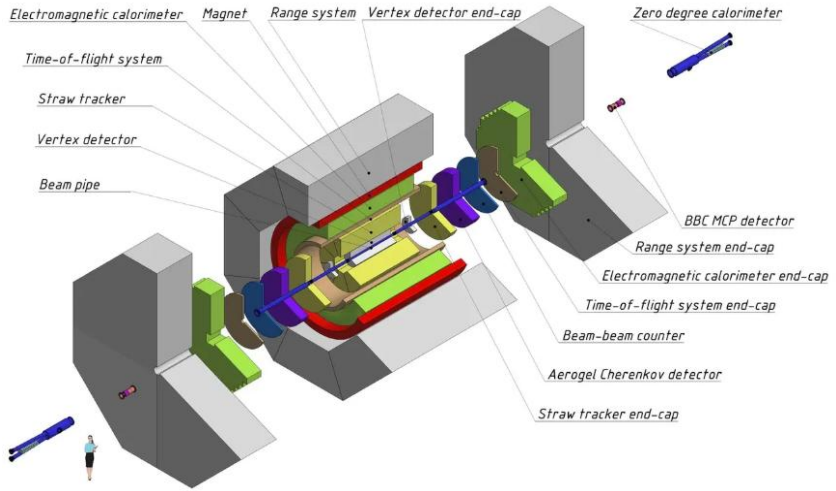
Detector sync clock: 125 MHz

Stage 1



Sub-detector	Num Ch	Ch/FEE	Num FEE
Micromegas	5384	128	43
Straw tracker	30512	64	478
BBC	1056	64	18
BBC MCP	64	32	2
Range system	137600	192	717
ZDC	210	64	34
Total (max)	**176716**		**1292**

Stage 2



Sub-detector	Num № Ch	Ch/FEE	Num FEE
Vertex DSSD/MAPS	***327680/12000***	***640/8***	***512/1500***
Straw tracker	30512	128	478
Calorimeter	27168	64	425
TOF	***12228***	***8***	***1529***
FARICH	***70144***	***64***	***1096***
BBC	1056	64	18
BBC MCP	64	32	2
Range system	137600	192	717
ZDC	210	64	34
Total (max)	**608552/283076**		**4811/5800**

Concept of triggerless DAQ for SPD

Why is triggerless?

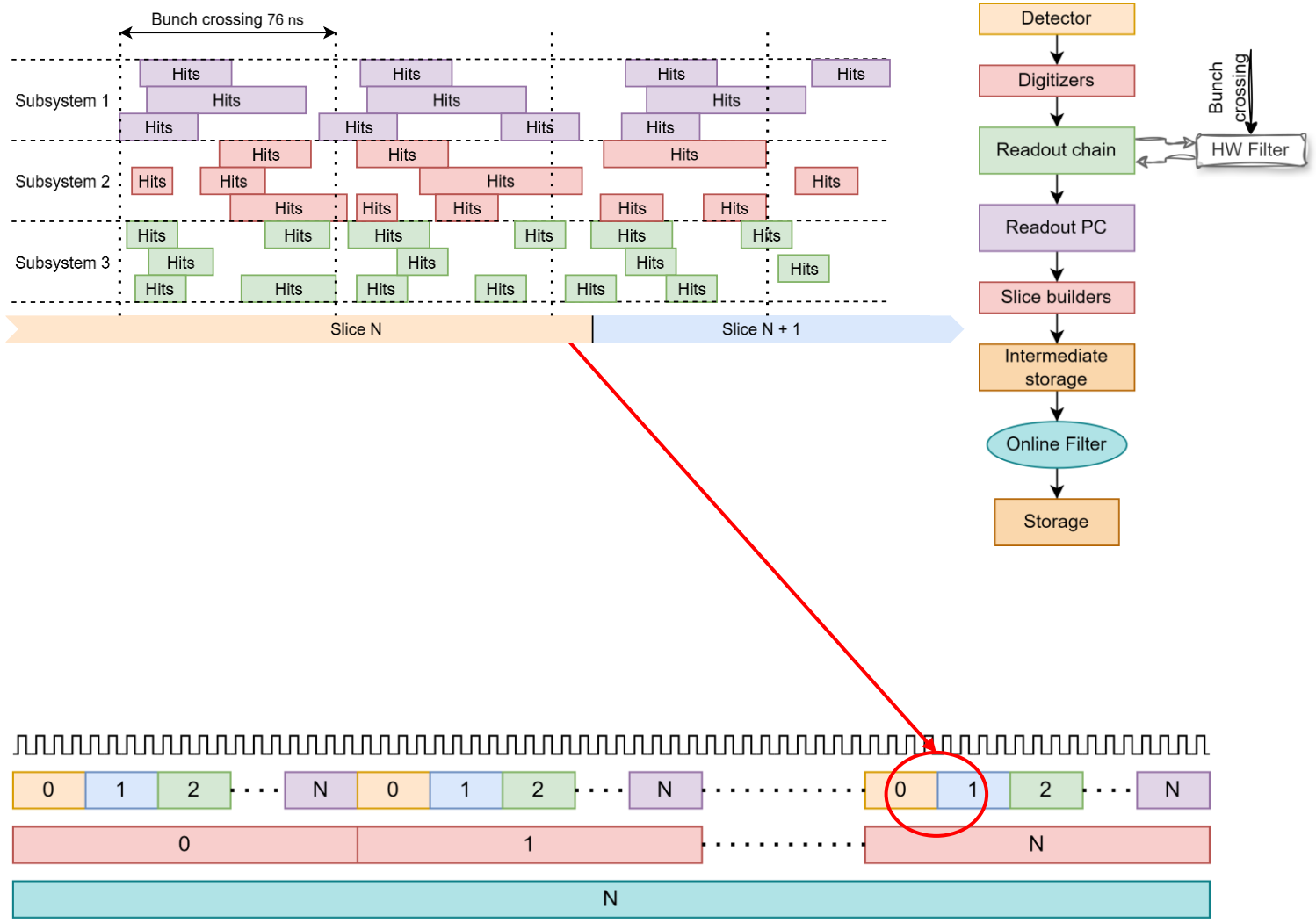
- Absence of a universal fast detector with 100% efficiency in identifying all potentially interesting events
- Broad physics program of SPD requires flexible event selection that cannot be predefined by fixed hardware trigger criteria

Time struct:

- Run: 0.5–10 hours
- Frame: 0.1–10 sec
- Slice: 10–100 μsec

Requirements:

- Each readout electronics is synchronous relative to the others
- The timestamp is recorded at the moment of digitization
- Electronics do not use RAM buffering; the FIFO* principle is observed
- Time continuity in the readout electronics within a *Frame*
- Control via synchronous/asynchronous commands



*FIFO - First Input First Output

DAQ Struct

Elements of DAQ:

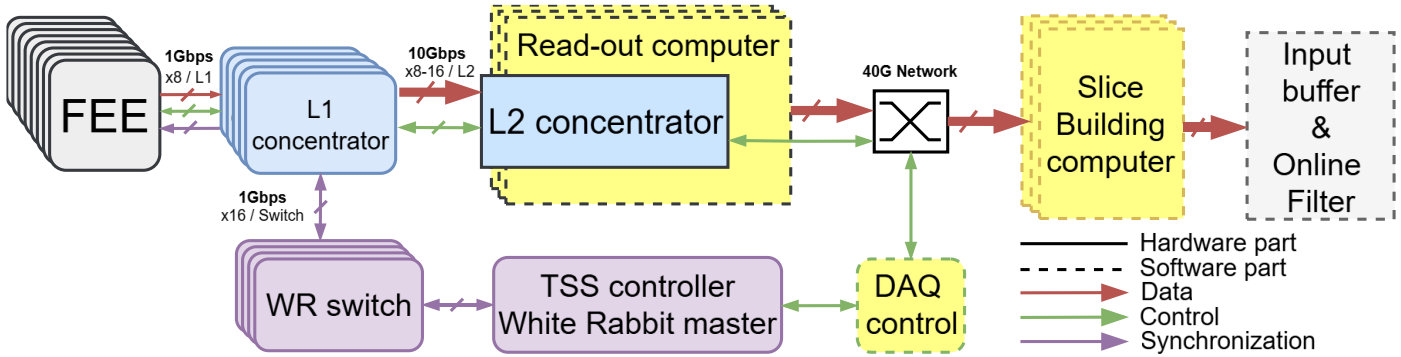
- Read-out chain
  - L1 – Level 1 concentrator
  - L2 – Level 2 concentrator
  - Read-out computer
- Time Synchronization System
- Slice building system

SPD Stage	Read-out (FEE) electronics Data links	L1 (8 ports)	L2 (16 ports)	Read-out PC	Slice Builders
First	~1292	>165	>12	>6-12	>5
Second	~5800	>730	>50	>25-50	>40

- Packet-based data transmission between all system components.
- Standardized interfaces and communication protocols for all components.
- Multiple access paths to every element of the readout chain.

Bandwidth per one link:

- FEE-L1: **1.25 Gbps**
- L1-L2: **10 Gbps**
- Read-out computer – Slice building system: **40 Gbps** or more



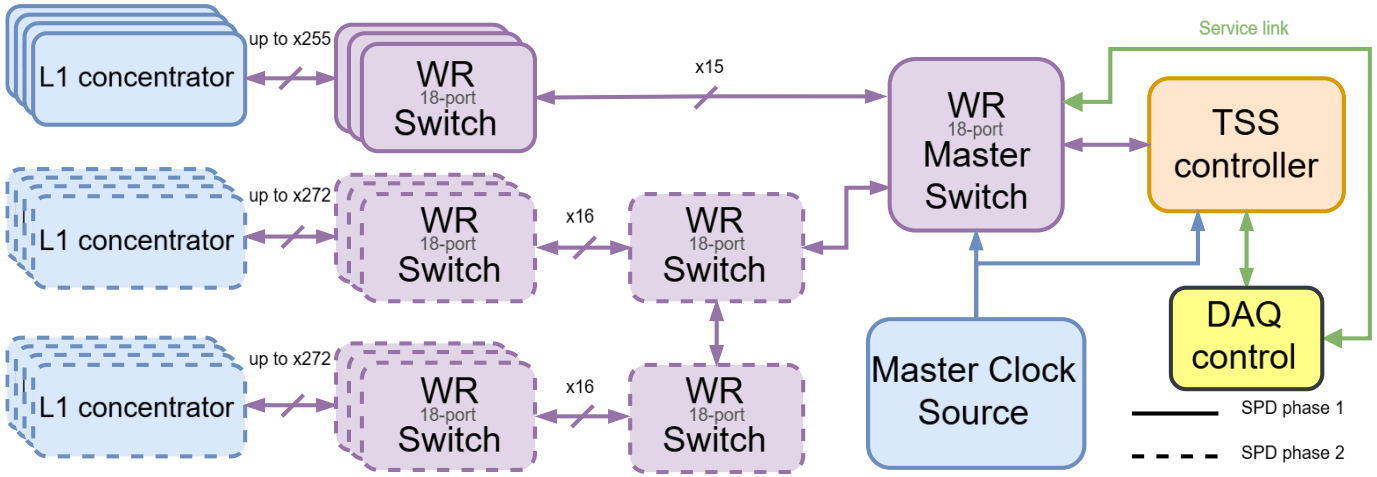
Synchronization (WR network)

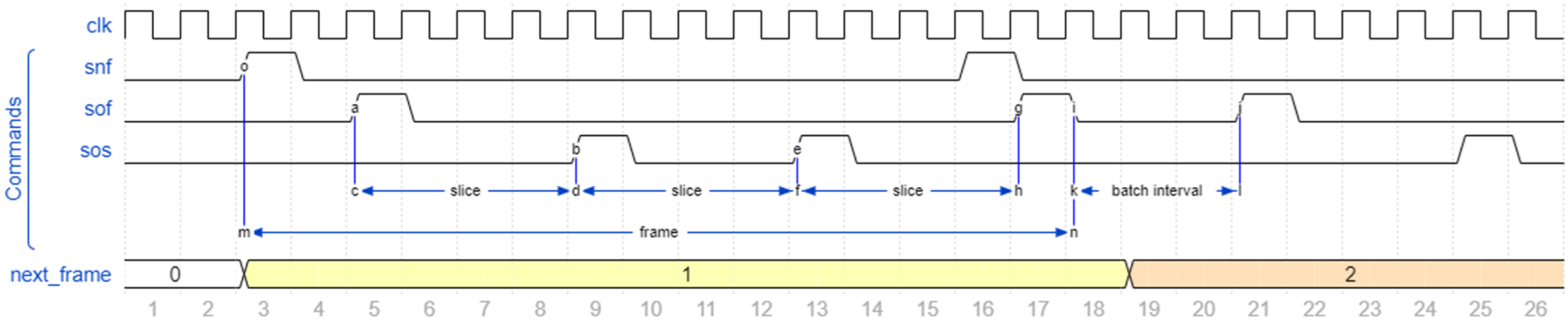
Time synchronization system tasks:

- Generation and distribution of a 125 MHz clock frequency with an accuracy of better than 1 ns and a jitter of better than 50 ps (TDR requirements)
- Generation and distribution of synchronous commands to the detector

Components:

- TSS controller
- Ultra-stable clock source
- 18-port White Rabbit switches
- White Rabbit *node* is integrated into L1 concentrator





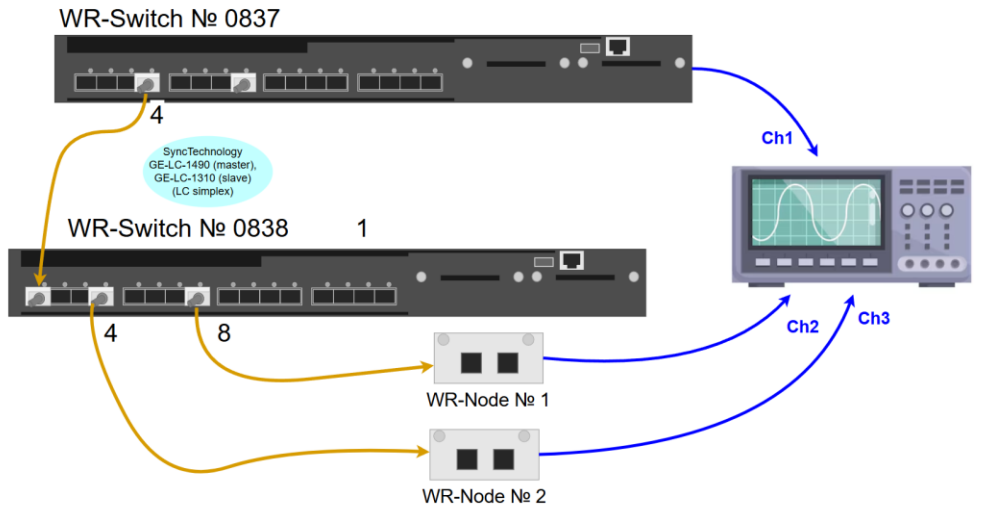
Synchronization (Test)

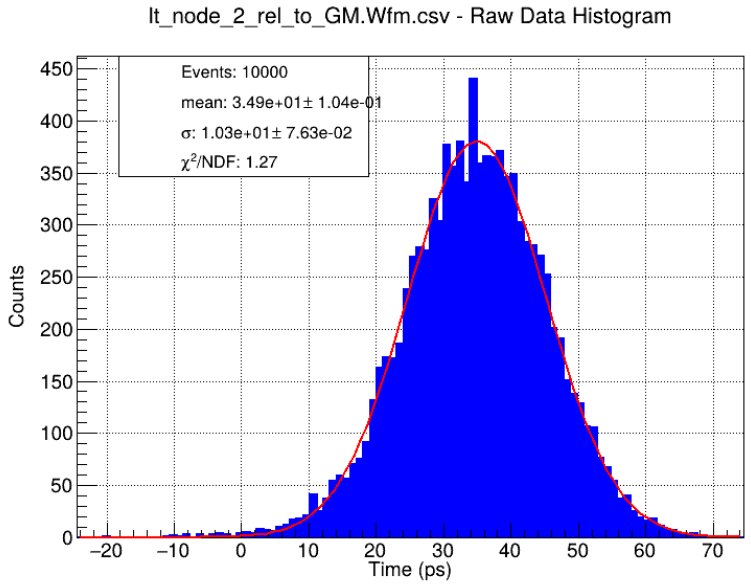
Measured:
- Delay between master and nodes
- Delay between nodes

Measurements were taken on the output PPS (Pulse Per Second) signal
Results are repeated after resets

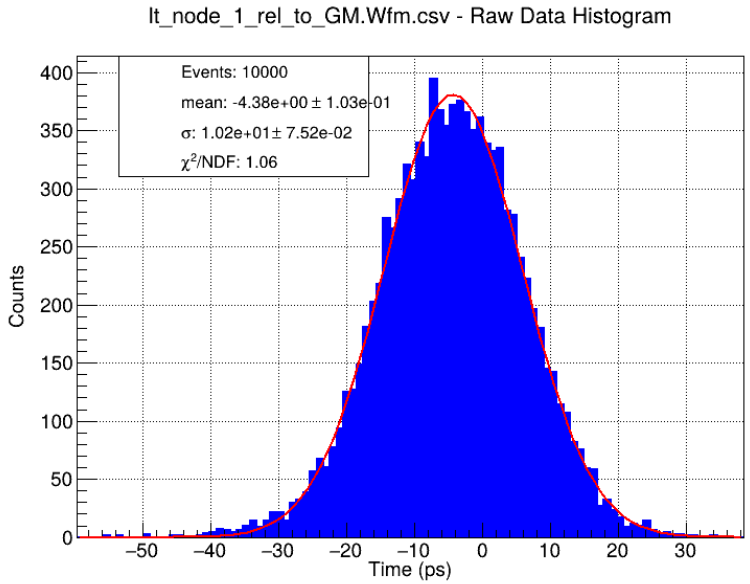
It is possible to estimate the PPS phase deviation from the reference and jitter

Measurement	Skew (mean)	Jitter (σ)
Node №2 & Master	34.9 ps	10.3 ps
Node №1 & Master	4,38 ps	10.2 ps
Node №2 & Node №1	39,3 ps	6,1 ps

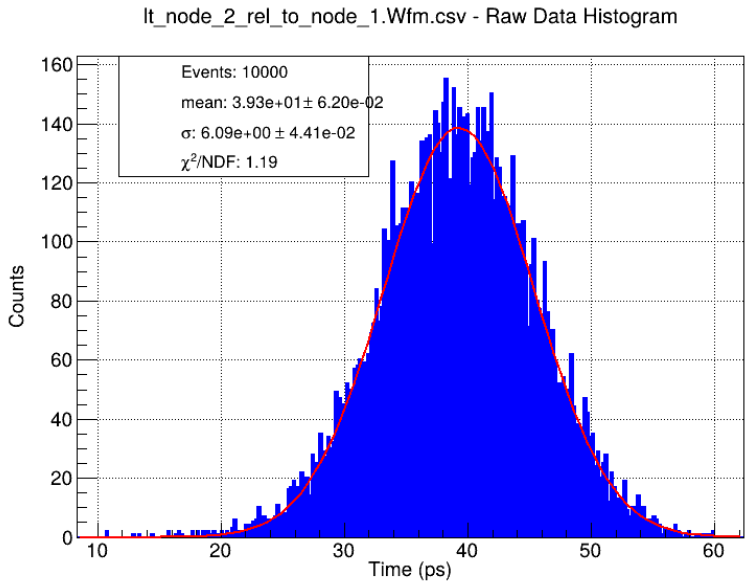




Node №2 & Master



Node №1 & Master



Node №2 & Node №1

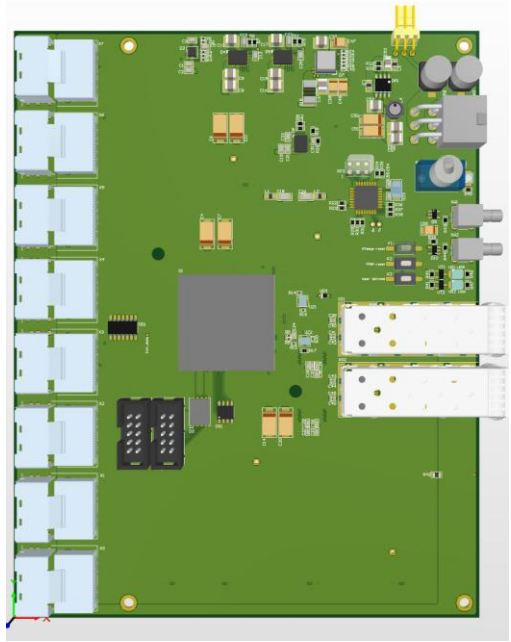
L1 concentrator (hub)

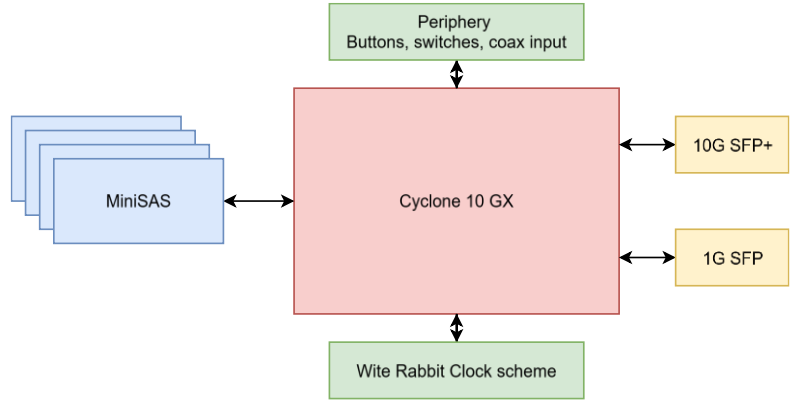
Hardware:

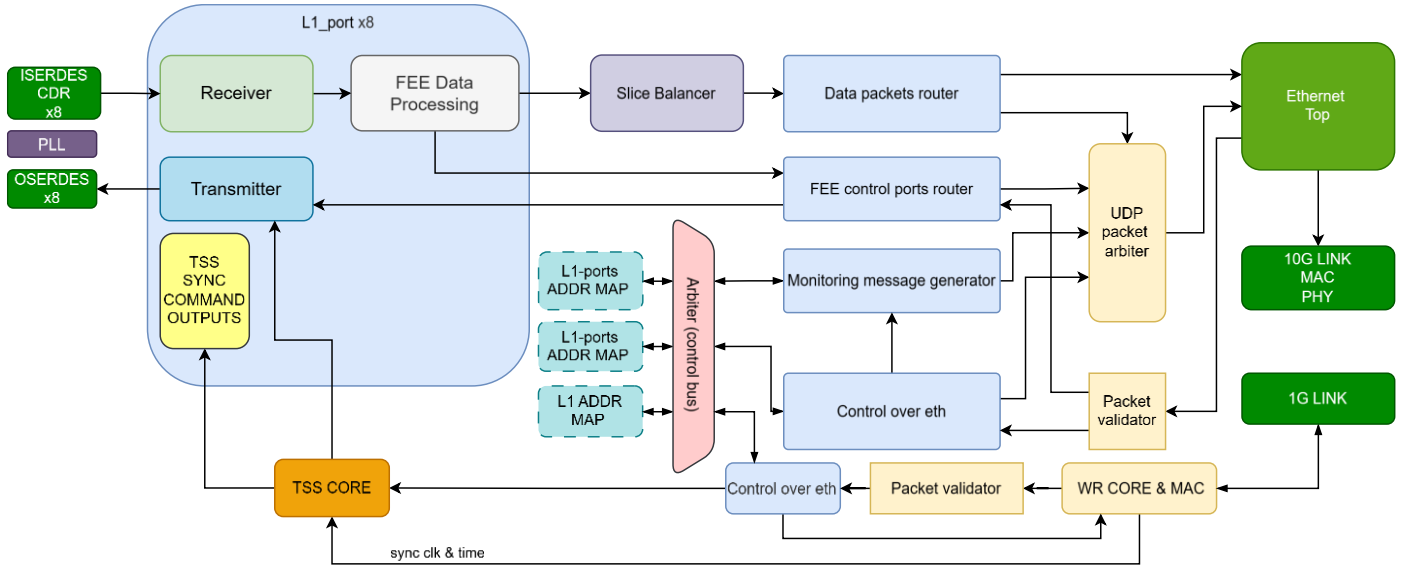
- Cyclone 10GX (105YF780E6G)
- 8x Links for connect FEE (miniSAS connectors for example) 8 diff pairs per connector
- SFP+ 10Gb transceiver for data transmission to L2
- SFP+ transceiver for TSS (White Rabbit)
- 1.25 Gbps link between FEE and L1

Tasks:

- FEE* data collection, data integrity monitoring, data flow monitoring
- FEE operation management (start/stop, resets)
- FEE status monitoring
- Reception and distribution of global clock signal and commands from the TSS controller
- FEE reconfiguration and FEE firmware update







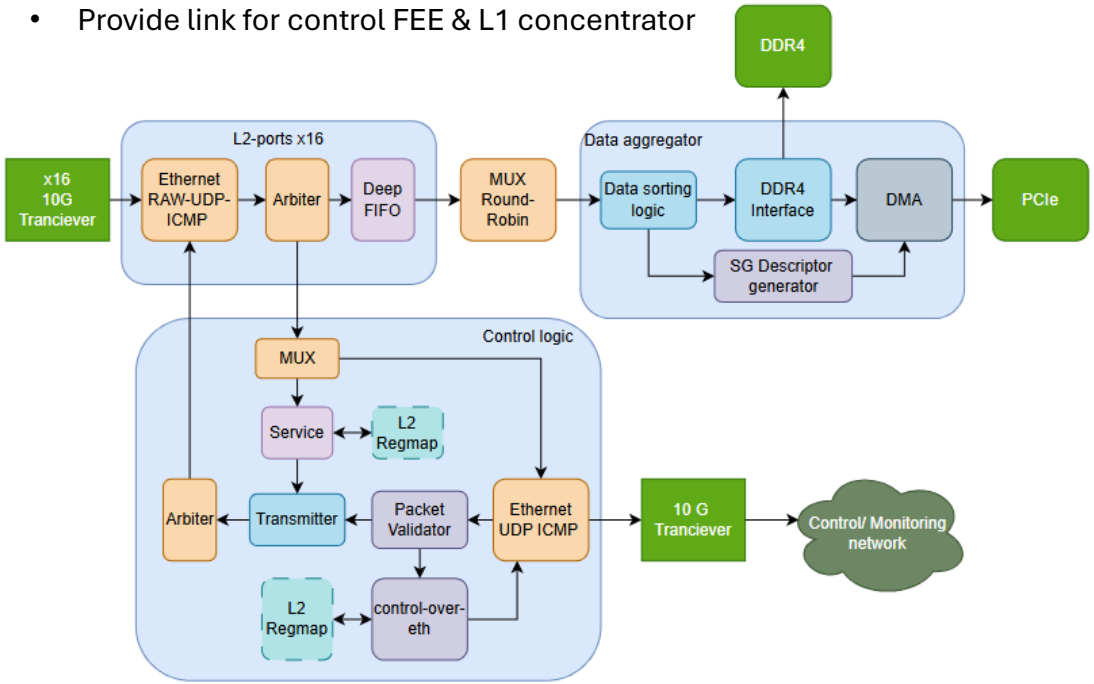
L2 concentrator (hub)

Hardware:

- Kintex Ultrascale+™ XCKU15P (FPGA SoM)
- Up to 16 10G optical links for L1-L2 channel
- PCIe® Gen3 ×16
- 1/10G link for control/monitoring network

Tasks:

- Data aggregation, Data integrity monitoring, Data flow monitoring
- Data preprocessing (FEE data sorting by Time Slice)
- Provide link for control FEE & L1 concentrator

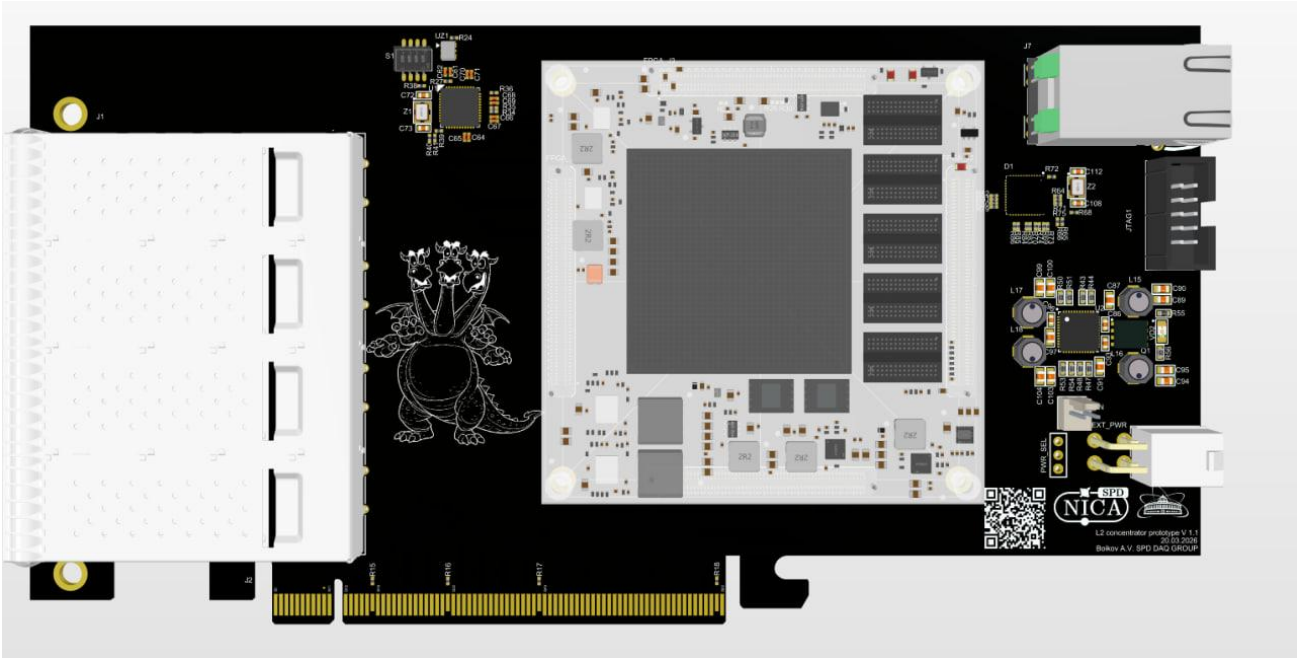


- ACKU15 FPGA SoM with AMD Kintex Ultrascale+™ XCKU15P
- 10 GByte (80-bit) DDR4 SDRAM
- 1 x PCIe® Gen3 ×16
- Dimension: 80 x 80mm form factor
- Gigabit transceivers
  - 32 x GTH, up to 16.3 Gbps
  - 24 x GTY, up to 28.21 Gbps



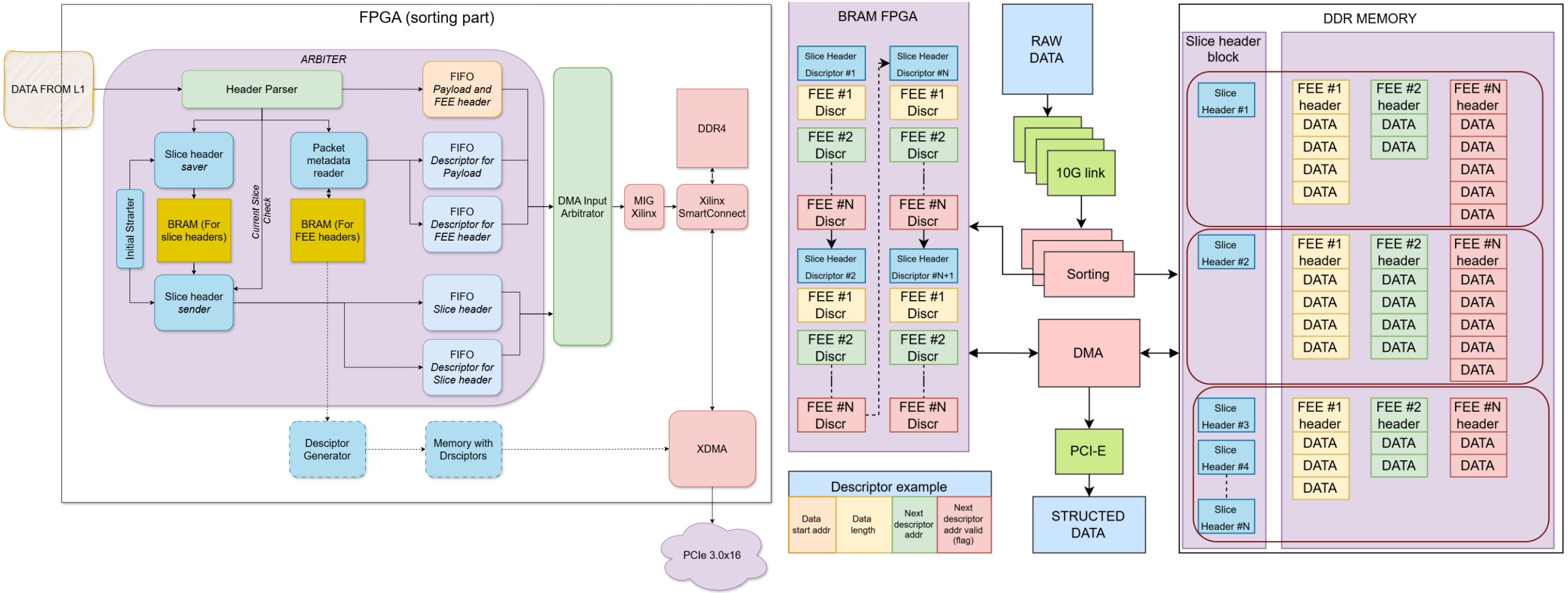


QSFP to 4 SFP converter



L2 concentrator (hub) sorting

- One slice header for all FEE 1-256
- Delay 8 Slices before start transfer process over PCIe.



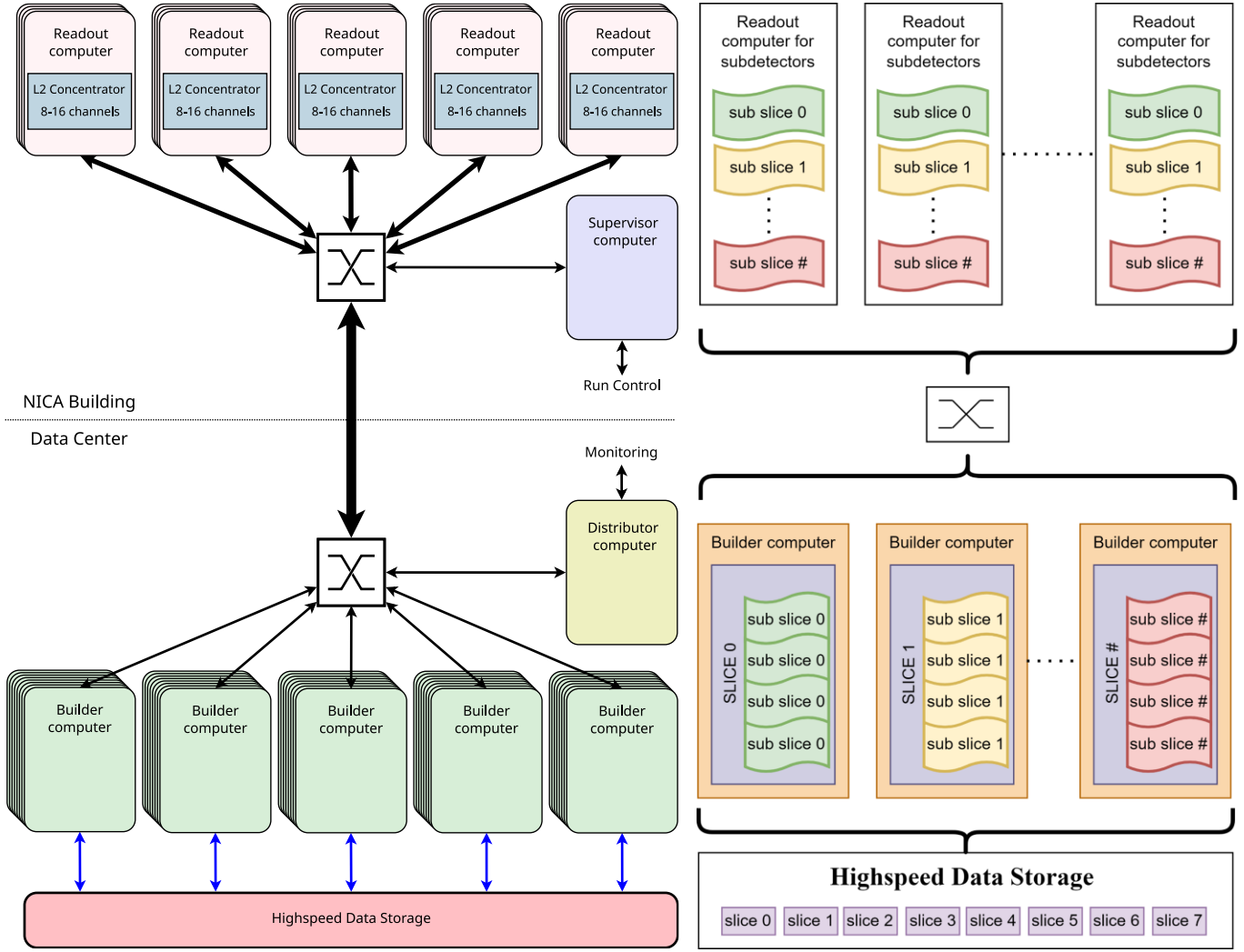
Slice building system

Tasks:

- The primary function of the slice-building system is to combine sub-slices from each readout computer into a unified data structure for subsequent processing by the online filter.
- Additionally, the system can provide detector groups with access to raw data (sub-slices) for monitoring.

Elements:

- Read-out-PC – Acquisition of a sub-slice from each detector system
- Builder – Merging sub-slices and forming a unified data structure
- Supervisor – Arbitration of the slice-building system
- Distributor – Provision of raw data for monitoring



Monitoring and control

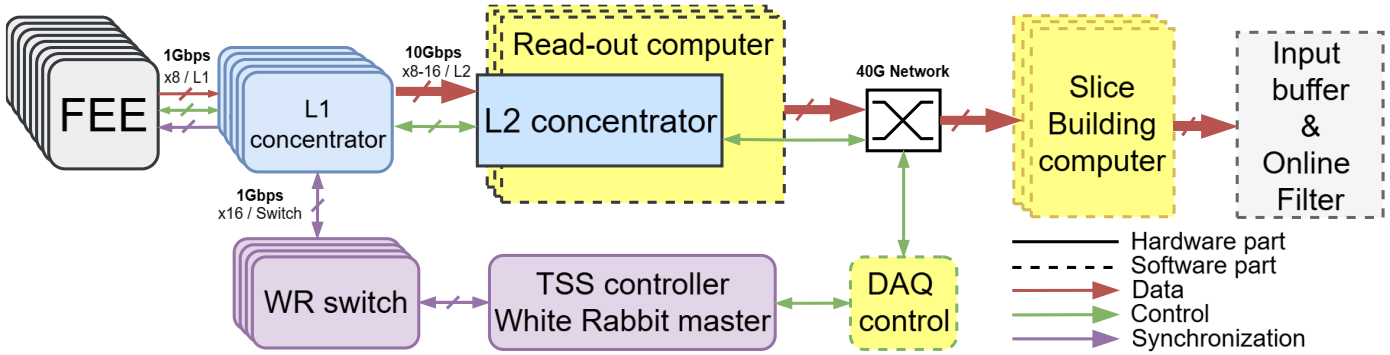
Base logic:

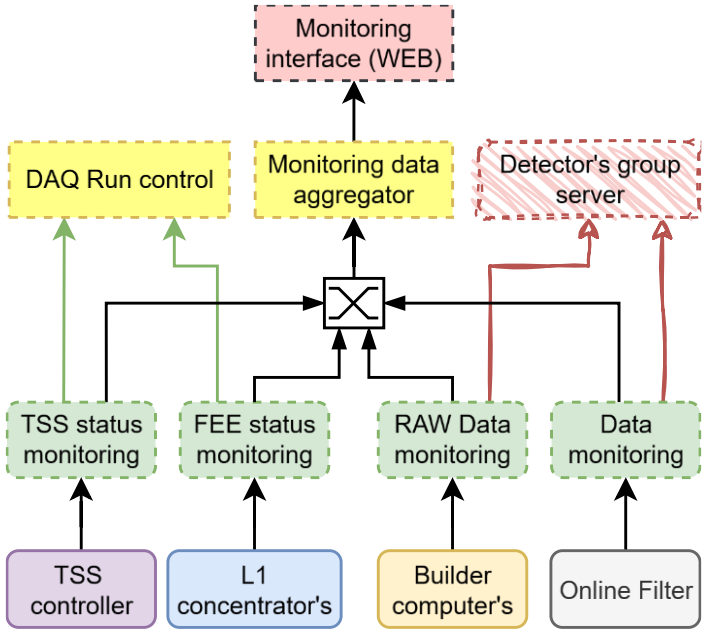
- The entire system is controlled via “DAQ Control”.
- Full FEE management is performed via readout chain.
- Each concentrator in network will be visible as a separate device.

Monitoring:

- FEE status and data volume from each FEE
- Data transmission errors
- Synchronization system status
- Raw data provision for detector groups
- .....

FEE and L1 status monitoring will be performed via a system of messages generated in the L1 concentrator.





Summary

- Triggerless DAQ architecture is designed to meet the requirements of the SPD experiment at NICA, with data rates more 20 GB/s (Stage 2).
- Precise time synchronization based on White Rabbit technology, providing a common clock and synchronous command distribution across the readout electronics.
- FPGA-based L1 and L2 concentrators performing data collection, integrity monitoring, buffering, and time-slice sorting.
- Modular and scalable architecture supporting the increasing number of readout channels and data throughput requirements of the SPD experiment.
- Experimental evaluation of the White Rabbit network demonstrating picosecond-level jitter and inter-node synchronization stability in the tested configuration.



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TSS test's

Achieved for a WR network of multiple switches:

- <80 ps PPS skew (after reset)
- <12 ps PPS jitter

Accuracy as average clock skew:

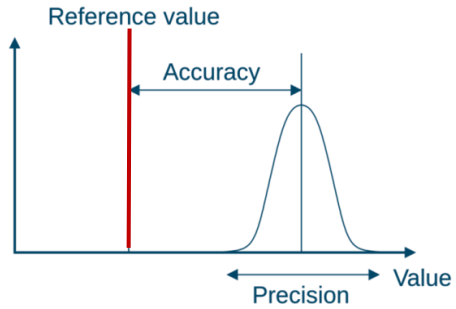
$$\overline{\Delta t} = \frac{1}{M}\sum_{i=1}^{M}(t_{ref} - t)$$

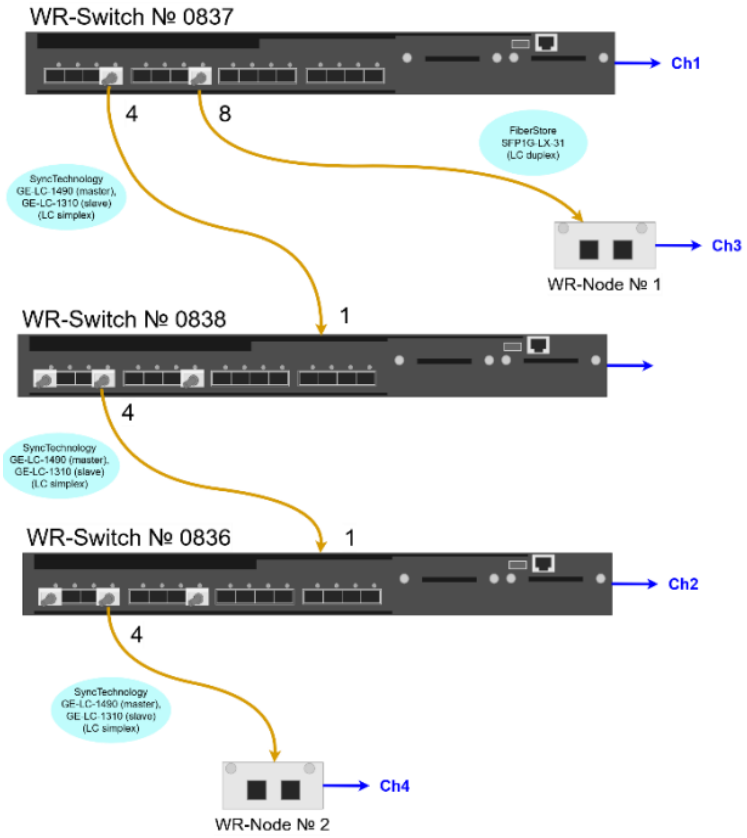
SPD requires: < 1 ns

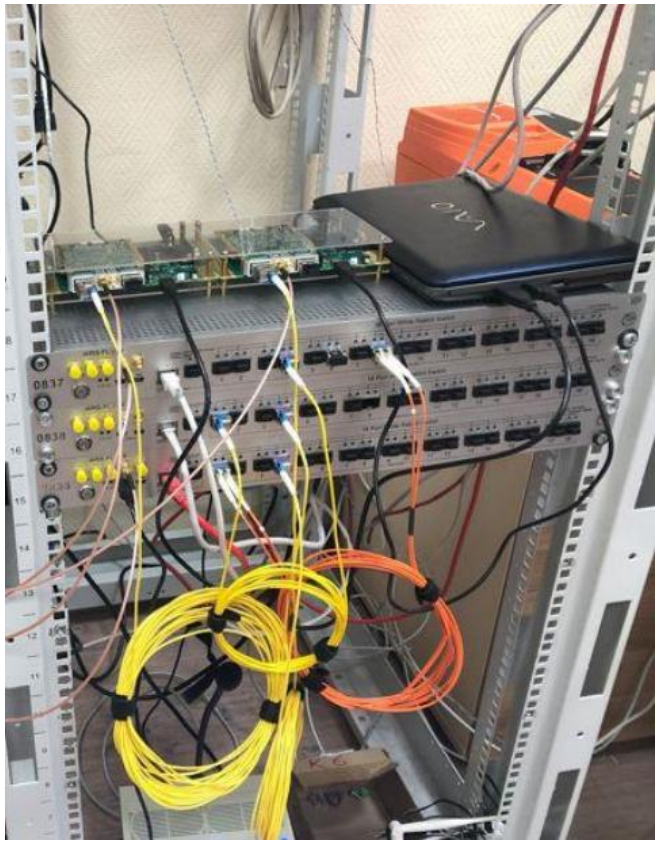
Precision as relative rms jitter:

$$\sigma_N = \sqrt{\frac{1}{M-1}\sum_{i=1}^{M}(\Delta t_i - \overline{\Delta t})^2}$$

< 50 ps







Temperature effect (claimed):
- 10 ps/°C skew error (2 ps/°C achievable)*
- Slight jitter error

Requires further verification for our system

* arXiv:1406.4223v1 (2014)