Передовые инженерные школы

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SPD NICA

White Rabbit Technology Evaluation for the SPD Experiment

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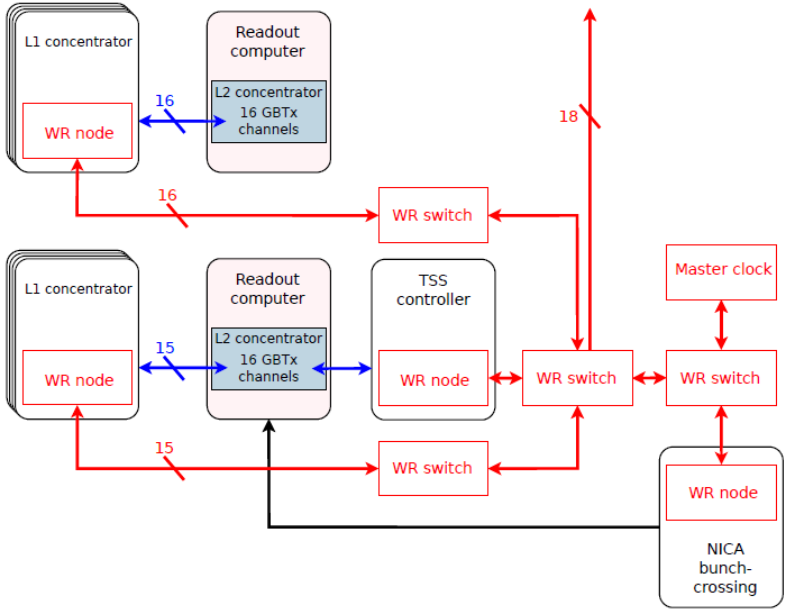
Presentation brief

- SPD experiment and TSS subsystem
- DAQ precision and accuracy requirements
- White Rabbit calibration
- White Rabbit precision and accuracy evaluation results

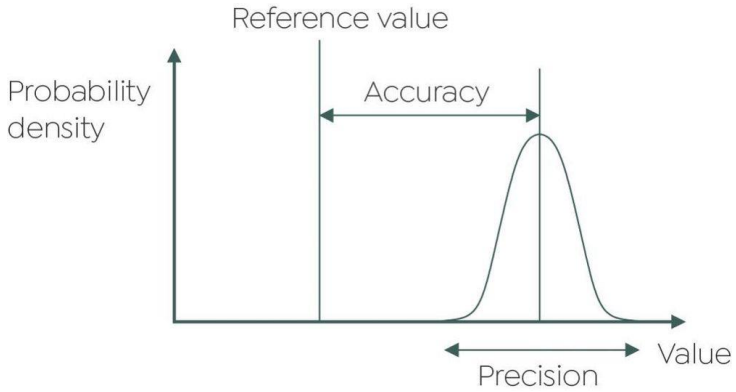
Time Synchronization Subsystem (TSS) with White Rabbit



1. **Provides the global clock and time** for the SPD DAQ
   - WhiteRabbit PTP (high accuracy profile of the IEEE1588-2019) – standard open protocol developed and maintained by CERN
   - Expected accuracy is better than 1 ns
2. **Generates and distributes synchronous commands** to mark data frames and slices
   - Run Control sends Start/Restart, Stop and Abort commands to TSS controller
   - The TSS controller generates a schedule
   - TSS nodes (at L1) receive this schedule and generate synchronous commands to front-end electronics

What is accuracy and precision

After initial synchronization WR node tracks the global clock and maintains the equal frequency of the local clock.



Accuracy as average clock skew:

$$\overline{\Delta t} = \frac{1}{M}\sum_{i=1}^{M}\left(t_{ref} - t\right)$$

Precision as relative rms jitter:

$$\sigma_N = \sqrt{\frac{1}{M-1}\sum_{i=1}^{M}(\Delta t_i - \overline{\Delta t})^2}$$

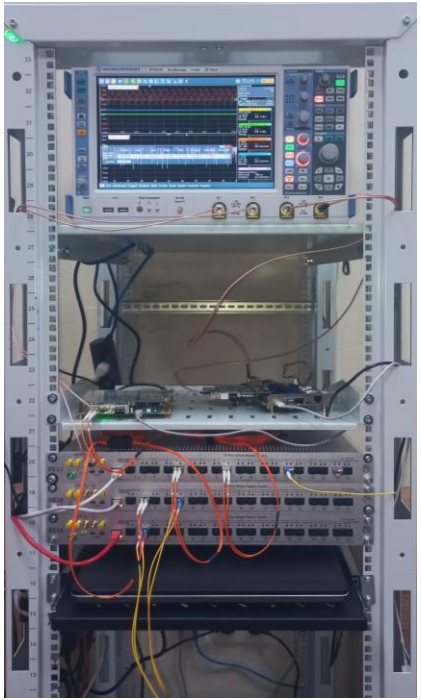
SPD requires:

< 1 ns

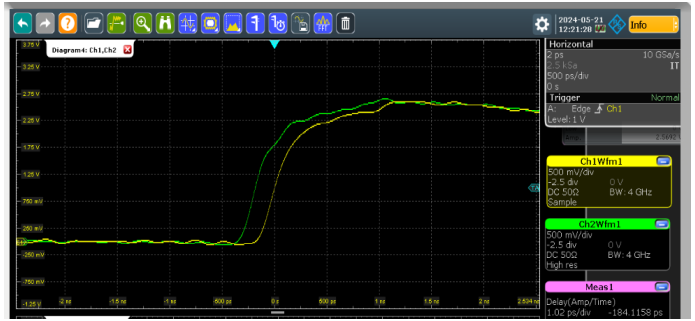
< 50 ps

- Sub-nanosecond accuracy can be achieved after calibration.
- Jitter depends on the hardware and environment.

Calibration



Calibration of WR devices significantly decreases relative skew between clock signals of calibrated devices.



Each different pair of devices' ports [and each cable type] should be calibrated

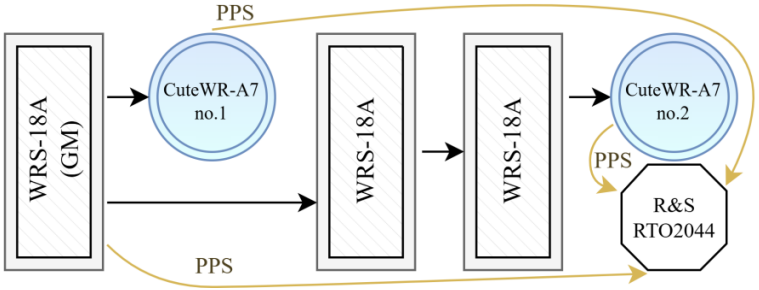
Measurements with Rohde & Schwarz RTO2044

- in room temperature conditions
- 20 GHz sample frequency

- Calibrated SyncTechnology WR switches and nodes
- Reference clock: 10 MHz clock from top-level WR switch's internal oscillator

Experiment setup and expected clk characteristics

SyncTechnology devices
RTO2044 Delay measurement function
Sampling mode: 20 GHz, linear interpolation
Signals: PPS (50% levels)

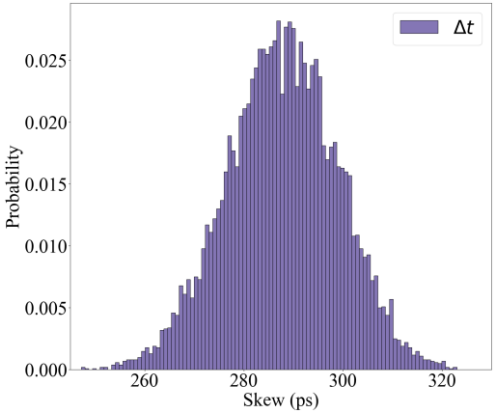


Required jitter measurement correction: 0.3-0.2 ps

$$\sigma_{Ncor} = \sqrt{\sigma_N^2 - \sigma_{ITJ}^2 - \left(\frac{\sigma_{IF_{SW}}}{S_{SW}}\right)^2 - \left(\frac{\sigma_{IF_N}}{S_N}\right)^2}$$

WR clk jitter
- has complex nature
- strongly depends on WR device implementation

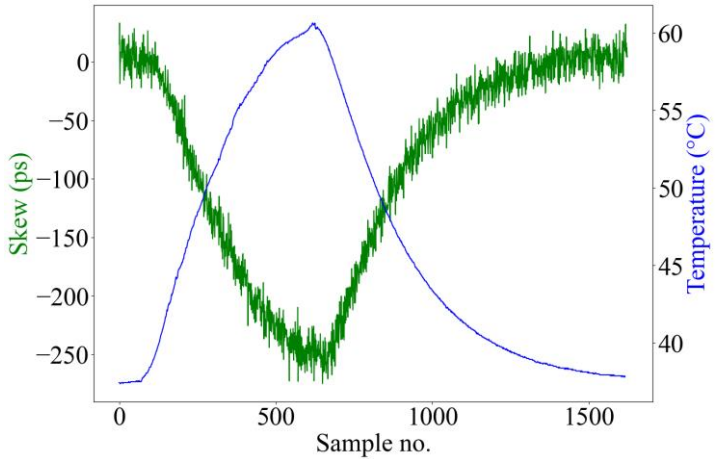
WR clk skew
- has a linear correlation with WR device temperature
- depends on complexity of factors
- depends on WR device implementation

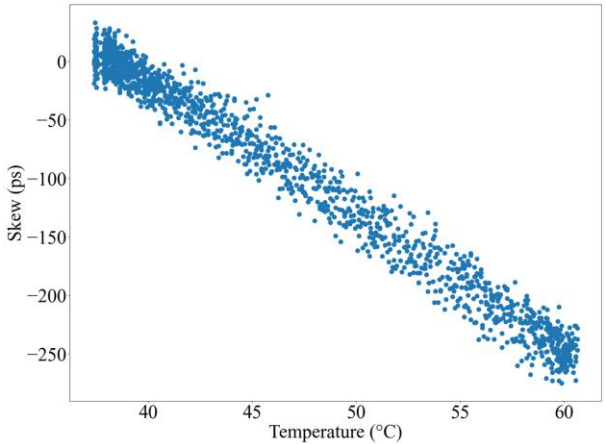


Temperature effects on clk skew
Slow temperature changes

WR devices will operate over the daily and seasonal temperature fluctuations.

Moderate slow temperature change (~30 min)
ΔT= (37-60°C), 260 ps Δt difference (11 ps/°C)





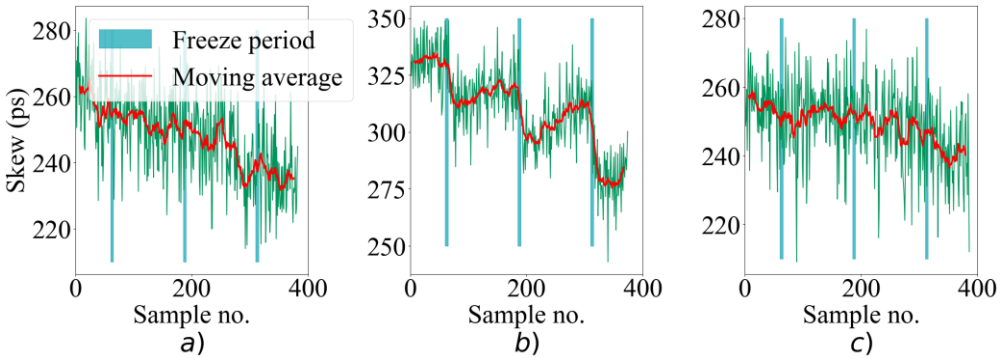
Pearson correlation coefficient
r = **-0,98700**

Temperature effects on clk skew (contd.)
Rapid temperature changes (-50°C)

Device: switch WRS-18
- Grand-master mode
- Fixed room environment
- Aerosol Freezer Spray
- Metal device case

Device: node CuteWR-A7
- Fixed room environment
- Aerosol Freezer Spray
- Heat sink, plastic case, SFP

Results: No significant changes in PPS skew

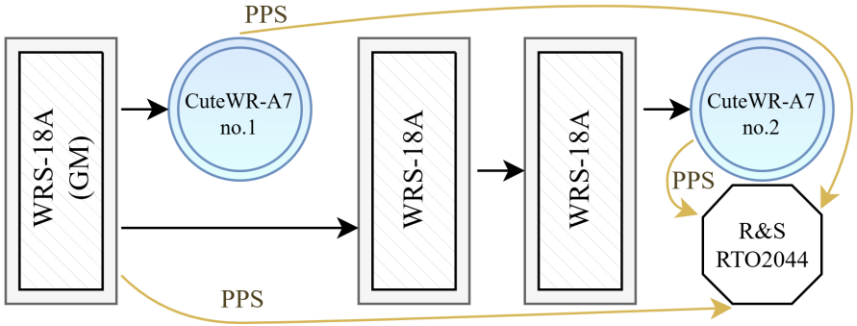


Results:
- rapid clk skew changes (~30 ps)
- long-term transient process

Conclusion: GM SW is protected from short-term weather effects

Conclusion: nodes are not protected from weather effects, but clk skew changes are tolerable

Temperature effects on clk skew (contd.)
Static temperature (20°C and 24°C)



- Eliminated long transient period

no. 1

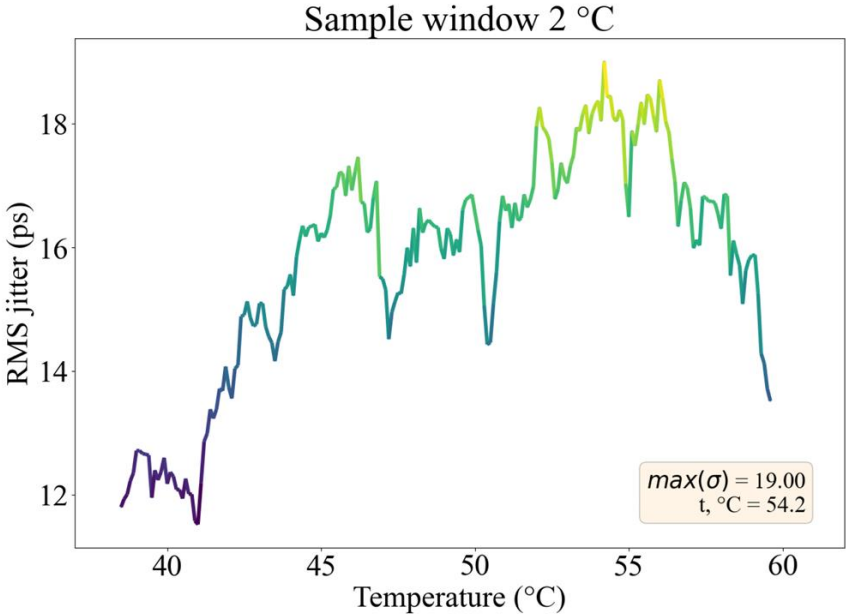
31 ps/°C skew error
<1 ps jitter difference

no. 2

1 ps/°C skew error
<2 ps jitter difference

Conclusion:
- unpredictable system-effects in the particular setup
- still tolerable clk skew

Temperature effects on clk jitter

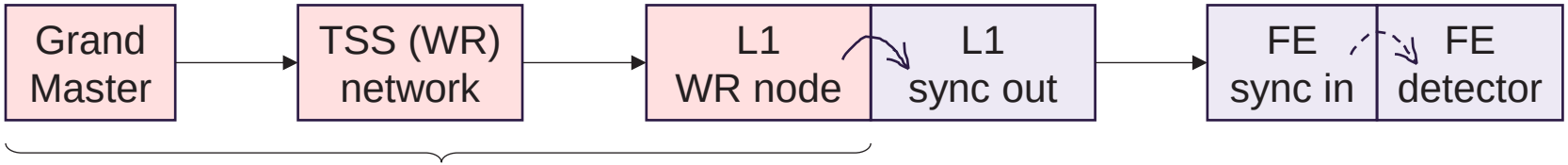


Very few reports on jitter and temperature correlation in the literature.

- **Device**: CuteWR-A7
- We have observed a jitter peak at 54.2°C
- The rise of the temperature leads to growth of the instability of the PPS signal

Conclusion: skew and jitter budget of a clock signal path

Different detectors may present more strict or more relaxed requirements.



SyncTechnology's WR provides acceptable baseline jitter and clock skew performance for SPD DAQ.

<300 ps PPS skew, <20 ps PPS jitter
Temperature effects: 30 ps/°C skew error, negligible jitter error

Future work for the TSS involves experiments and analytical estimates of accuracy and precision for the generated synchronous signals at the outputs of the SPD DAQ elements and their execution at the SPD detectors' side.

НАЦИОНАЛЬНЫЕ ПРОЕКТЫ РОССИИ

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