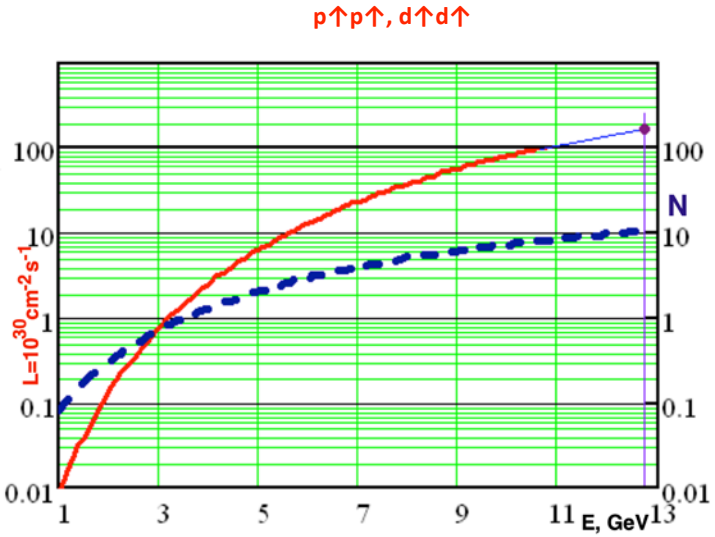
Planned free running DAQ for SPD experiment at NICA

Leonid Afnasyev on behalf of SPD DAQ group, JINR

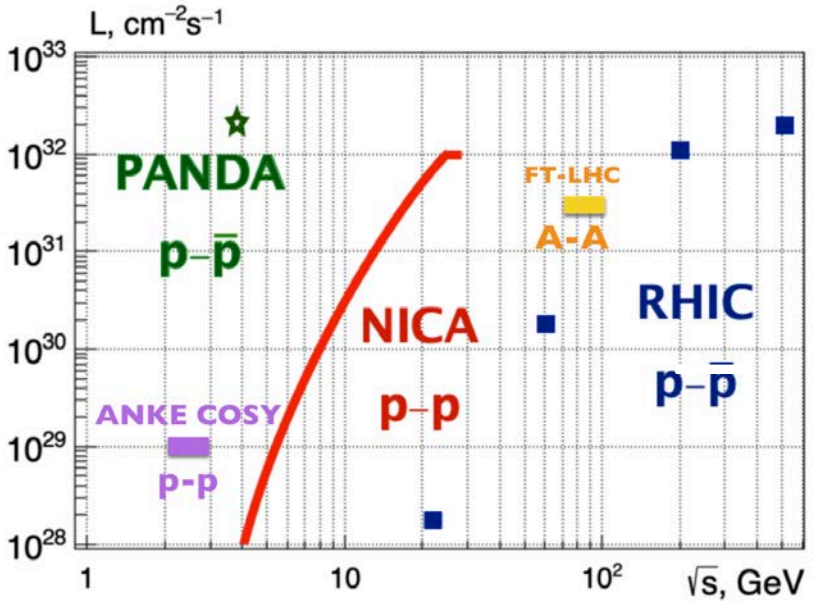
SCIENTIFIC GOAL OF THE SPD PROJECT



Main goal of the SPD experiment is to investigate the nucleon spin structure and polarization phenomena in collisions of longitudinally and transversely polarized protons and deuterons (|P|≤0.7) at center-of-mass energy $\sqrt{s}$ up to 27 GeV and luminosity L up to $10^{32} cm^{-2} s^{-1}$. Such probes as leptonic pairs, D-mesons, photons etc. are planned to be used for that.

HADRON STRUCTURE AND SPIN PHYSICS: MAIN PLAYERS / COMPETITORS

- **HERMES** (DESY, Germany) 1995-2007, e↑p↑, e↑d↑, $\sqrt{s} = 7.1GeV$
- **CLAS12** (Jlab, US) 2017 - …, e↑p, e↑d, $\sqrt{s} = 4.5GeV$
- **COMPASS** (CERN) 2002- …, μ↑p↑, μ↑d↑, πp↑, $\sqrt{s} = 17.3 - 19.4GeV$
- **STAR** and **PHENIX** at **RHIC** (BNL, US) 2002 - …, p↑p↑ $\sqrt{s} = 200,500GeV$
- **SeaQuest** and **SpinQuest** (Fermilab, US) 2012 - …, pA, pp↑ $\sqrt{s} = 15GeV$
- **AFTER@LHC** (CERN) 2025+, pp↑,pd↑, $\sqrt{s} = 115GeV$
- **future projects at EIC** (US) 2030+, e↑A, $\sqrt{s} = 20 - 140GeV$



SPD (JINR) 2025+,

p↑p↑,d↑d↑, $\sqrt{s} \leq 27GeV$

BRIEF HISTORY AND PRESENT STATUS OF SPD

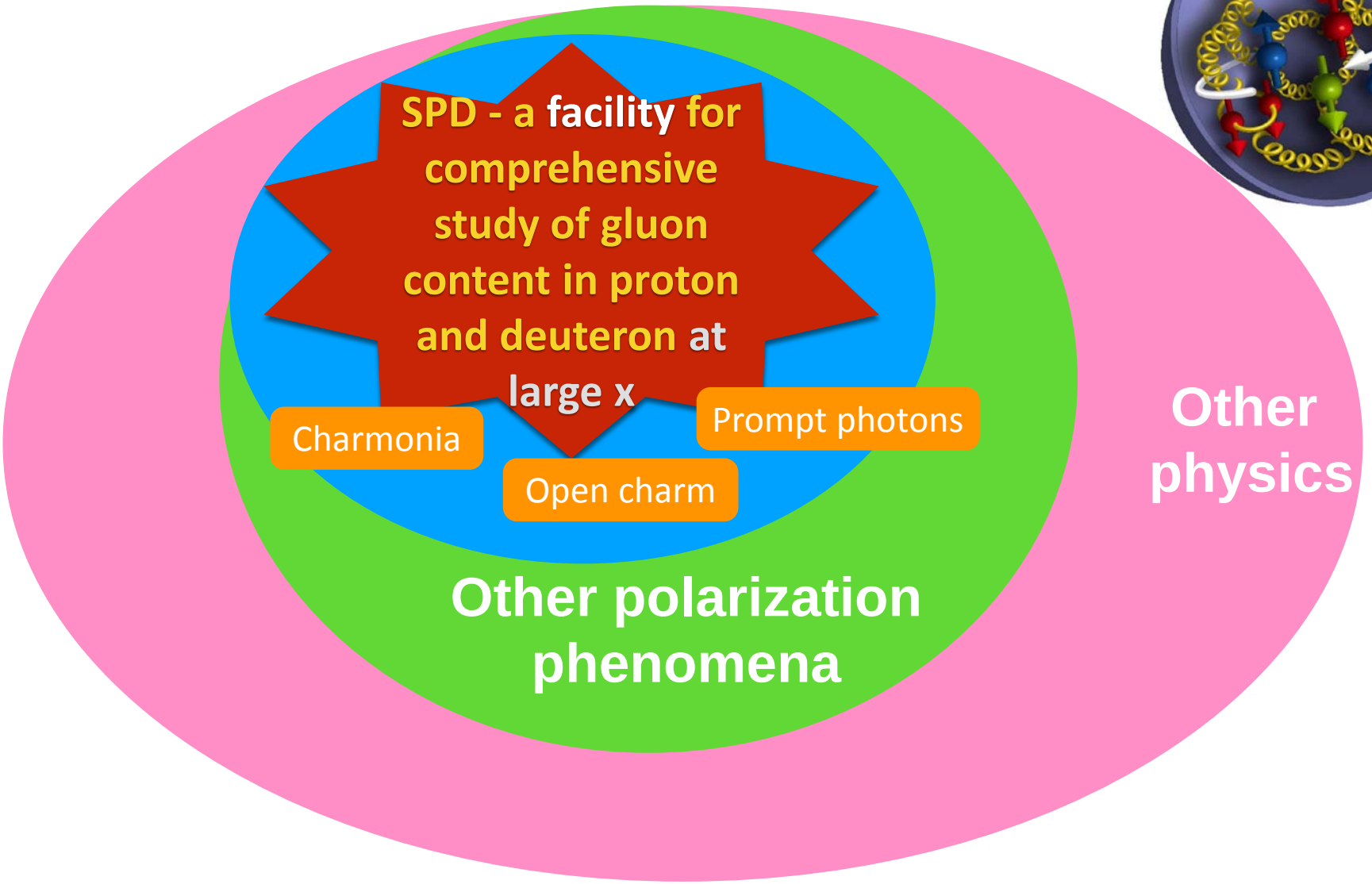
- 2007 — idea of the project, SPD was included as activity to the JINR topic plan.
- 2014 — Letter of Intent (approved by PAC)
- 2016 — SPD-oriented workshop in Prague
- 2018 — SPD-oriented workshop in Prague
- **2019 — SPD project is approved by PAC (till 2022)**
- 2019 — first proto-collaboration meeting
- **2020 — now we have:**

Preliminary physics program

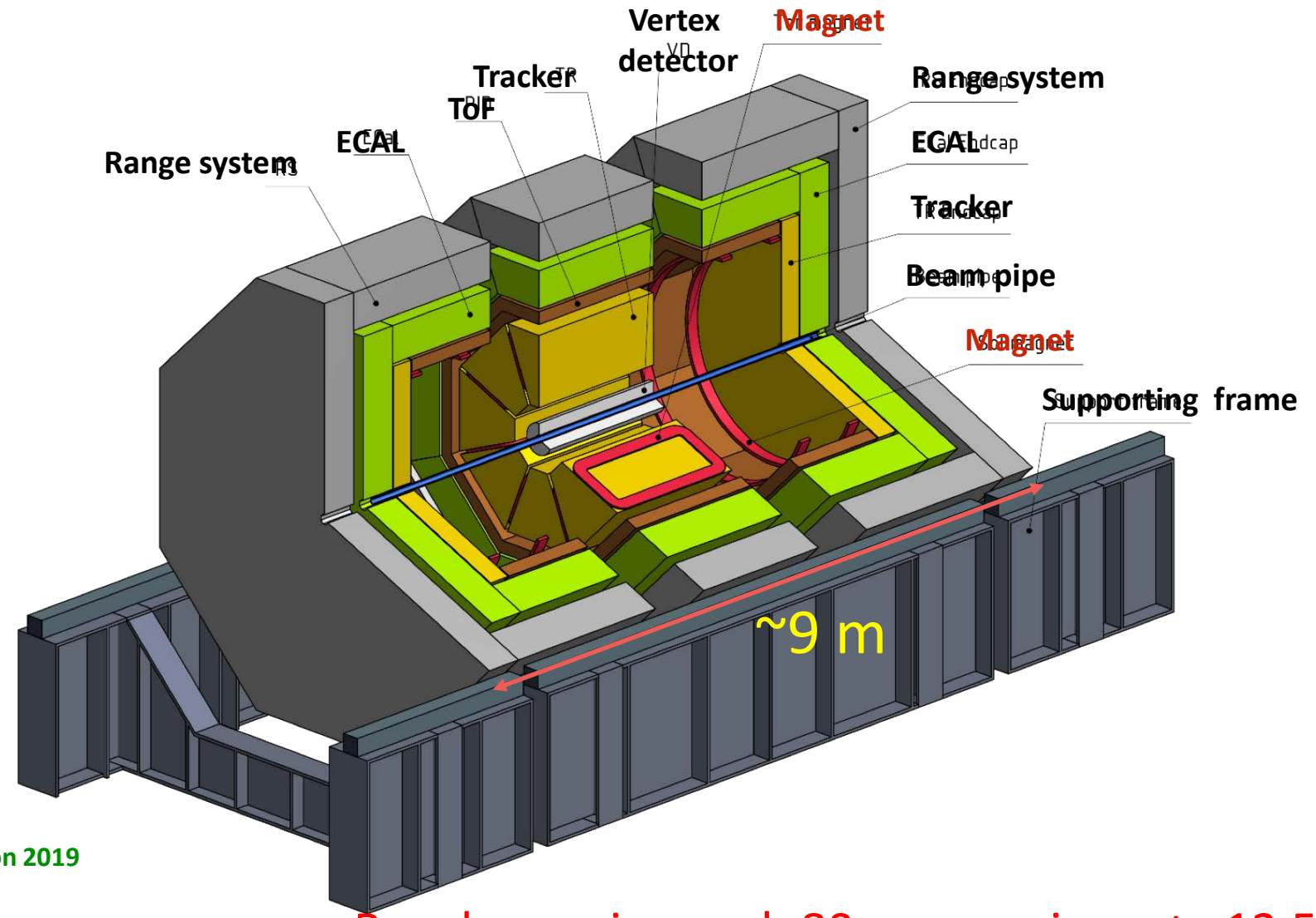
Preliminary concept of the detector

Groundwork for the main subsystems of the setup

CONCEPT OF THE SPD PHYSICS PROGRAM



CONCEPT OF THE SPD SETUP



Version 2019

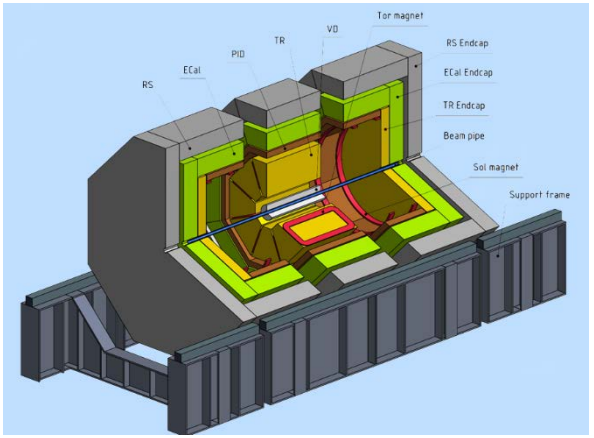
Bunch crossing each 80 ns; crossing rate 12.5 MHz,
Collision rate ~4 MHz Triggerless DAQ

Estimation of raw data flow *(preliminary , very rough!)*

Data flux was estimated for the maximum luminosity L = 10^{32} $cm^{-2}c^{-1}$ and maximum energy √s = 27 GeV.
At these conditions the event rate within the SPD aperture is $3 \cdot 10^6$ 1/s *(from old PYTHIA simulation)*.

Simplifications used in estimation of the data flux:

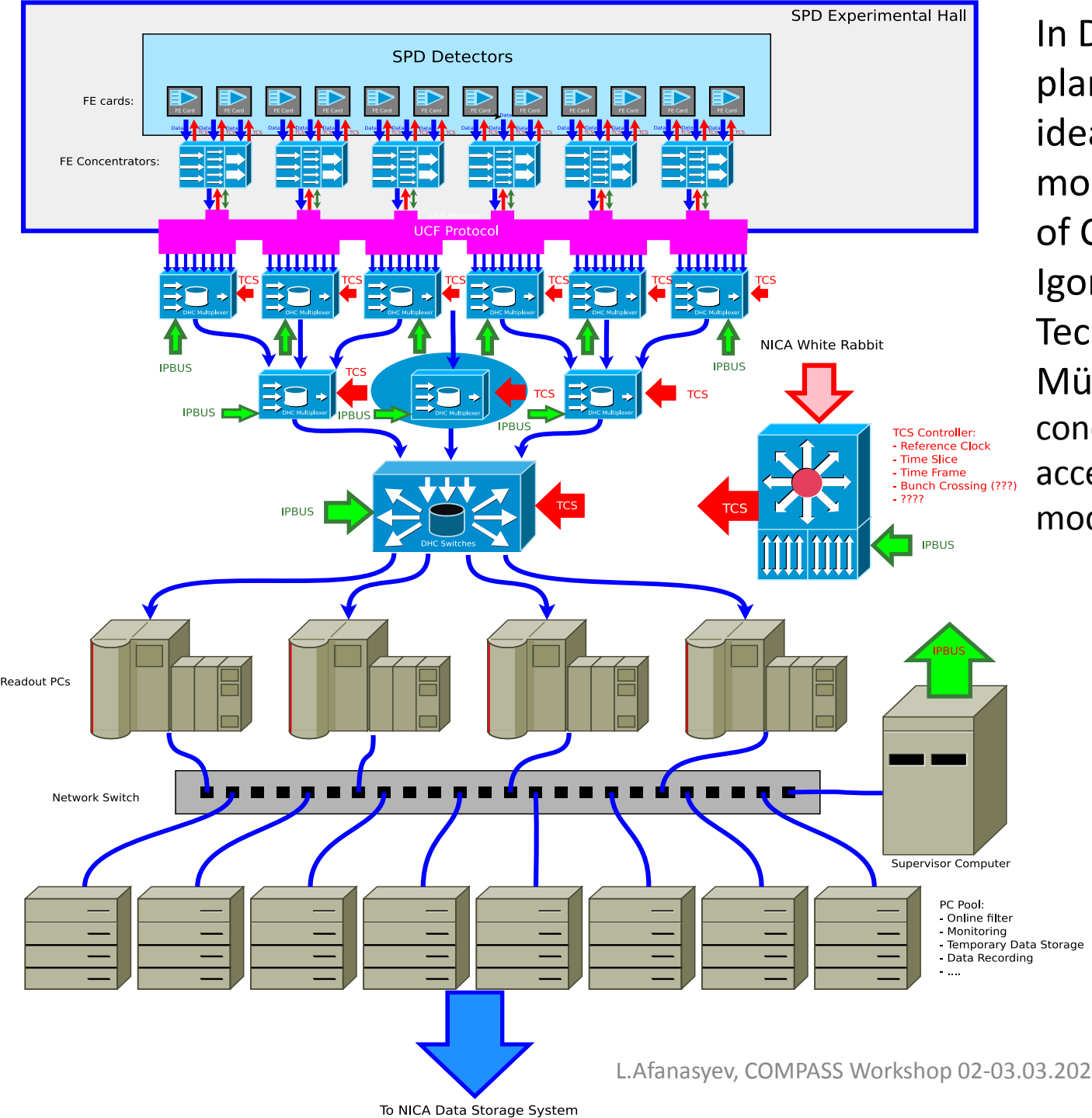
- all detectors have 100% detection efficiency for charge particles
- γ-quanta are detected only in ECAL, other detectors are transparent
- no double hits in a cell
- no noise signals, no background
- zero suppression implemented
- no headers, no calibration data etc.



Multiplicity values were obtained from simulations.

When appropriate, some numbers were taken from simulations of MPD and PANDA and from beam tests of these facilities.

With these approximations and with some safety margin the data flux is estimated as 20 GBytes/s.



In DAQ of SPD we are planning to employ the ideas developed for the modernized DAQ of COMPASS by Igor Konorov from the Technische Universität of München (TUM). His conception of SPD DAQ is accepted with minor modifications.

Front-end electronics for the free-running DAQ-SPD

Front-end electronics of the detectors has to meet the requirements of a free-running DAQ

General FEE requirements from the DAQ system *(preliminary)*:

- Self-triggered (*trigger-less*) FEE operation
- Digitizing on-board
- Zero suppression
- Large memory to store the data accumulated in a time slice
- Timestamp included in the output format

Front-End electronics for free running DAQ

- Silicon vertex detector – TDC/ADC: few promising options is developing for PANDA front-end electronics. No final decision yet.
- Electromagnetic calorimeter (SiPMs) – ADC: No final decision yet.
- Straw tracker – TDC: iFTDC developed for COMPASS, NA64 is planned for SPD.
- Range system – TDC: The SPD range system closely follows the design of the range system of PANDA, which is in a well-advanced state. The digital part of the PANDA front-end electronics is very closed to what we want for the SPD-DAQ.

Thank you for attention

Time stamping

In order to build the events from signals accumulated in a time slice, the data from each detector should be provided with a timestamp. For this purpose in SPD the White Rabbit system can be employed.

White Rabbit

Ethernet-based solution for sub-ns synchronization and deterministic, reliable data delivery

In NICA the White Rabbit system (developed at CERN) is used which provides synchronization for large distributed systems with timestamping of 125 MHz,
sub-nanosecond accuracy and ~10 ps precision.

White Rabbit allows one to time-tag the measured data and hence to group the hits to events on the timing base.

SPD-DAQ architecture

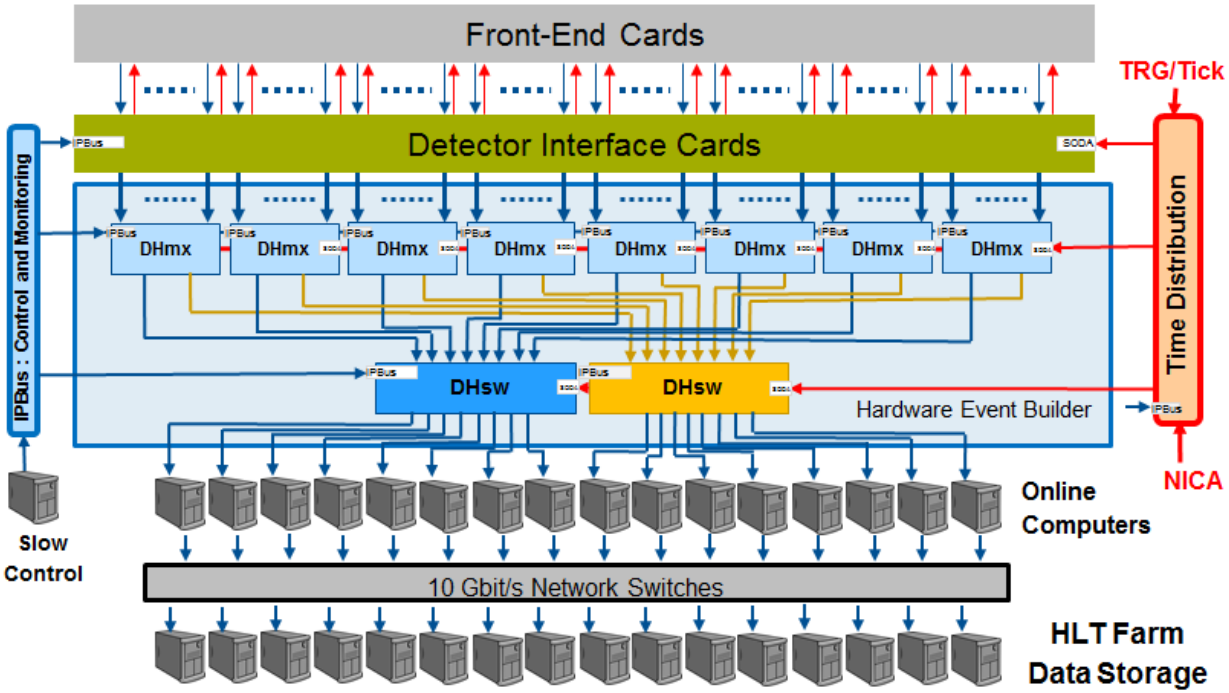
In DAQ of SPD we are planning to employ the ideas developed for the modernized DAQ of COMPASS by Igor Konorov from the Technische Universität of München (TUM) who is the coordinator of the DAQ-COMPASS.

In October 2018 he has sent us for discussion his proposal on DAQ for SPD:
“Data Acquisition System for the Spin Physics Detector”.

In his proposal the programmable FPGA chips are widely used in the DAQ structure.

This proposal can be taken as a base for building of the SPD-DAQ.

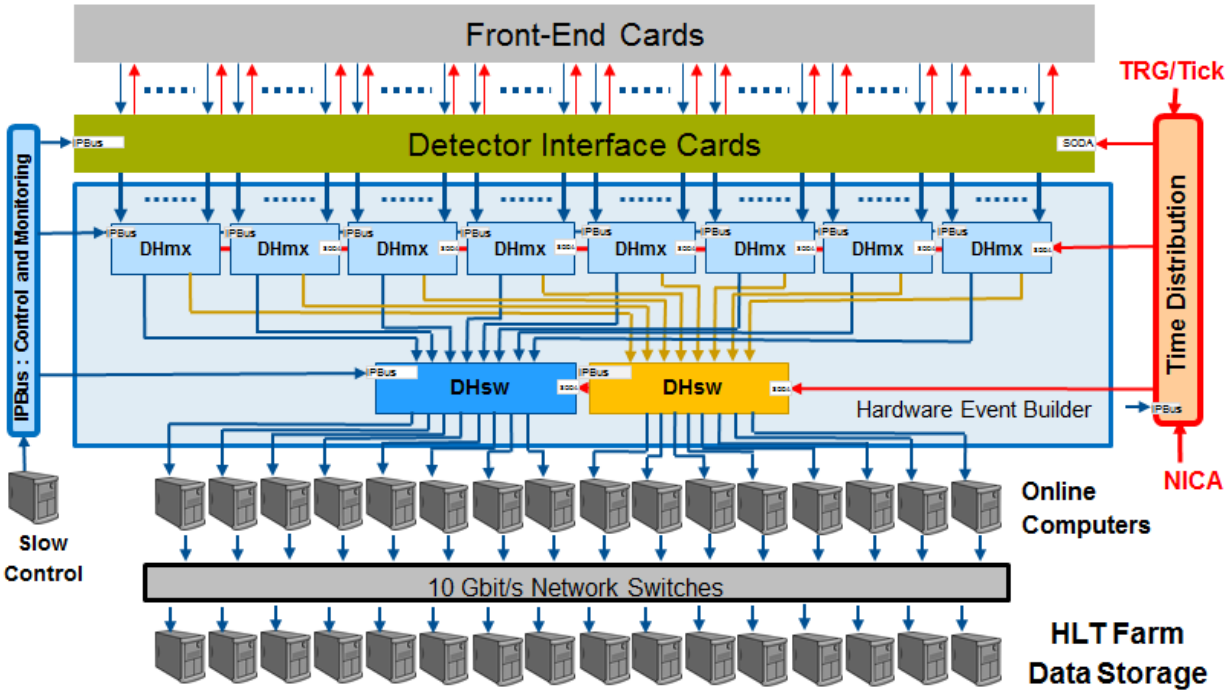
SPD-DAQ architecture *by Konorov*



Slow control accesses FEE via the detector interface cards (DIC) using UDP-based IPBus protocol.

DIC retransmit clock signals to FEE and convert detector information to a high speed serial interface running over an optical link. UCF (*Unified Communication Framework*) protocol will be a standard high speed link protocol within the DAQ.

SPD-DAQ architecture *by Konorov*

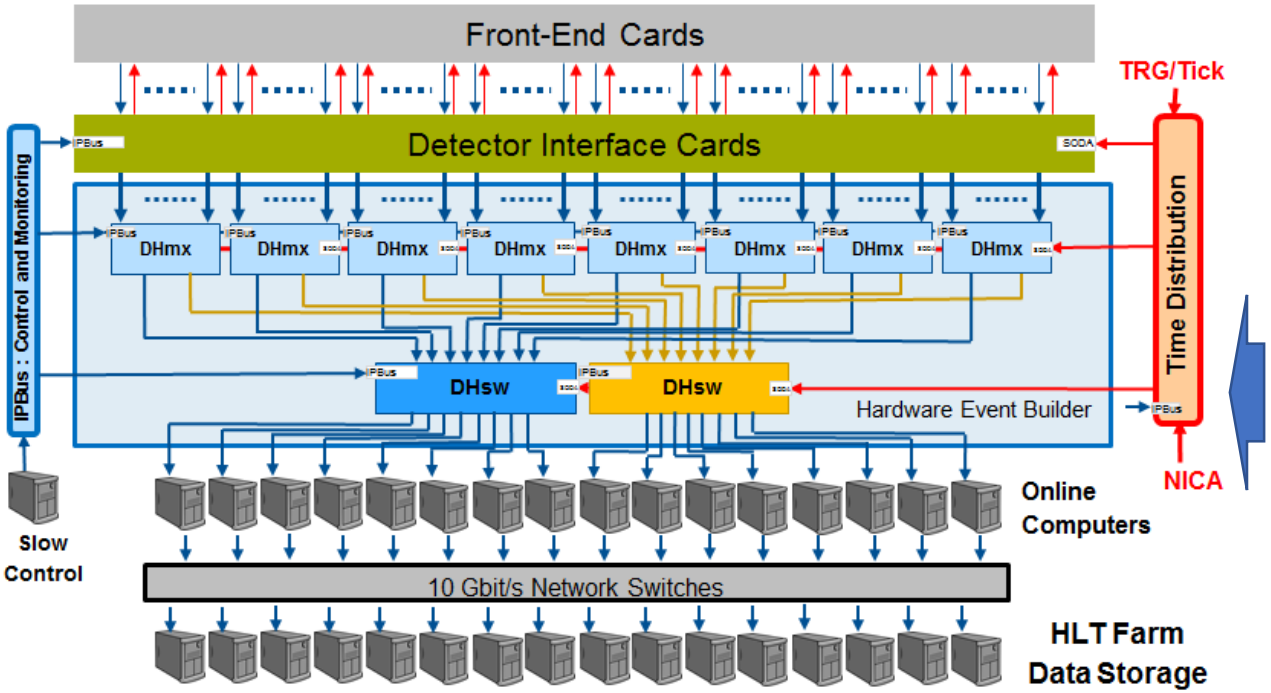


The multiplexer (DHmx) modules receive detector information via serial links, verify consistency of data, and store them in DDR memories.

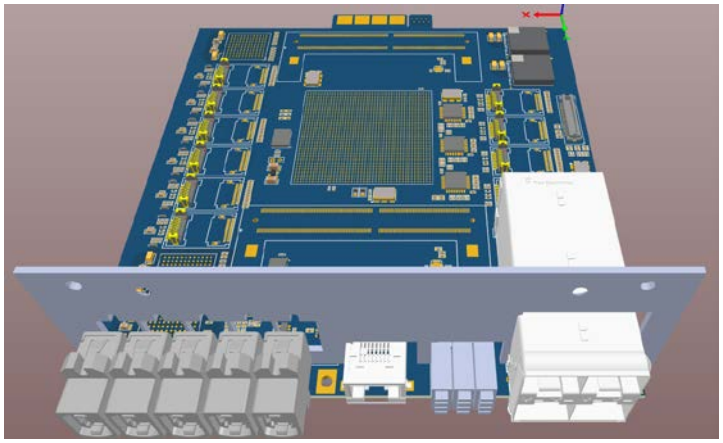
The multiplexer is equipped with 32 GBytes of memory.

All accepted data are assembled in sub-events and distributed to two switches.
Each multiplexer has a bandwidth of 2 GBytes/s.

SPD-DAQ architecture *by Konorov*



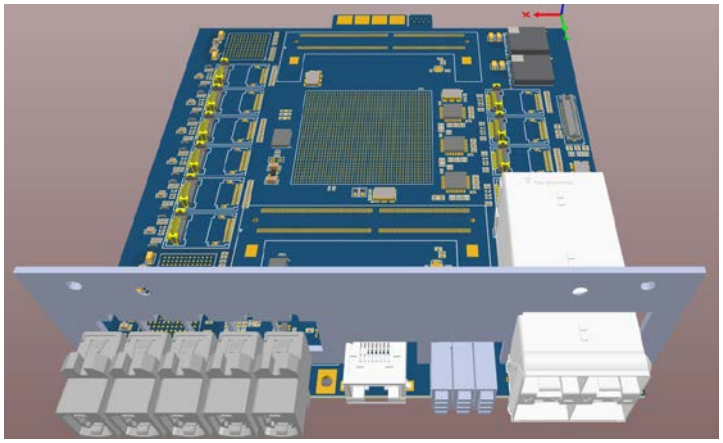
The switches (DHsw) perform the final level of event building and distribute the assembled events to 20 (?) on-line computers.



One and the same hardware **FPGA-based module** developed in TUM can be programmed either as a multiplexer or as a switch.

The multiplexer *DHmx* has 48 high speed input and up to 8 output interfaces.
A bandwidth of incoming interface can be programmed from 2 to 10 Gbps.
Outgoing interface runs at a fixed speed of 10 Gbps.

DHsw firmware functions as 10x10 switch and performs event building with a maximum throughput rate of 10 GBytes/second.



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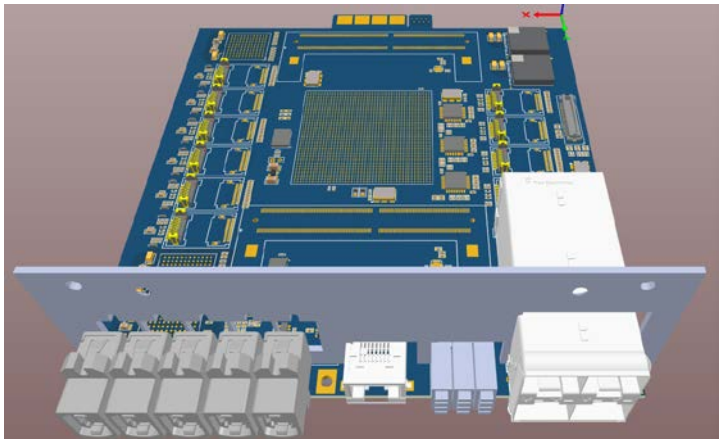
The whole system can be upgraded to much higher than 20 GB/s flux by implementing additional hardware *(that costs more money).*



We consider the proposal of Konorov as a good solution for the SPD-DAQ.

At the same time we are not obliged to follow it literally, and do not throw away the option of combining it with more traditional approach (not 100% FPGA-based).

One and the same hardware FPGA-based module developed in TUM can be programmed either as a multiplexer or as a switch.

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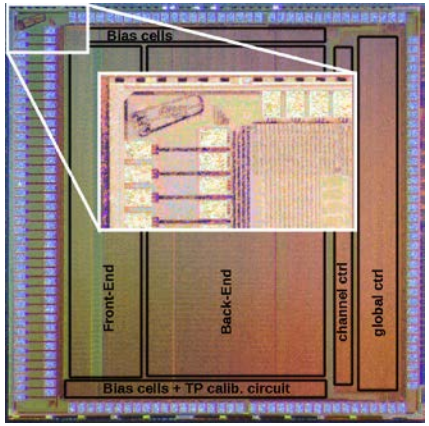
Vertex detector

In Turin the electronics based on the **TIGER** chip (Turin Integrated Gem Electronics for Readout) is developed for trigger-less readout ***of the GEM detectors***.
Charge and time measurements provided.

TIGER parameters

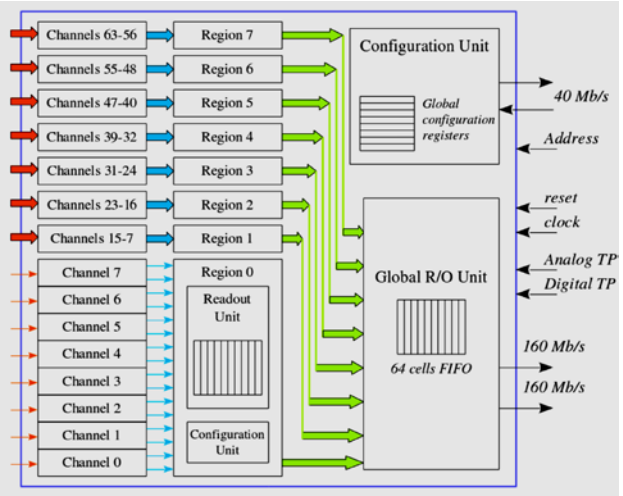
5 x 5 mm^2 110nm CMOS technology
64 channels: preAmp, shapers, TDC/ADC, local controller
Digital backend inherited from TOFPET2 ASIC (SEU protected)
On-chip bias and power management
On-chip calibration circuitry
Fully digital output
4 TX SDR/DDR LVDS links, 8B/10B encoding
Nominal 160 MHz system clock
10 MHz SPI configuration link
Sustained event rate > 100 kHz/ch



Vertex detector

Another project in Turin: **ToASt** (Torino Amplifier for Strip detectors).
Time and charge measurements provided.

Developed for the PANDA MVD strip detector readout

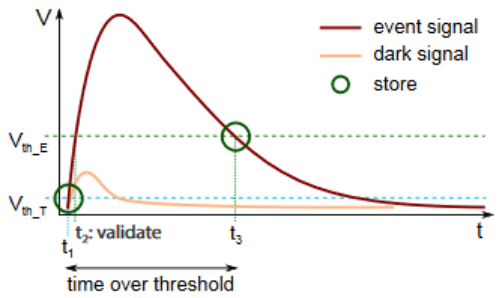


Some parameters:

- 64 input channels
- Time of Arrival (ToA) and Time over Threshold (ToT) measured
- master clock frequency 160 MHz
- 2 output serial links at 160 Mb/s
- charge resolution 8 bit
- time resolution (r.m.s.) 1.8 ns

Vertex detector

For the microvertex detector of PANDA a dedicated chip **PASTA** *(PAnda STrip Asic)* is being developed to be used in a free-running DAQ.



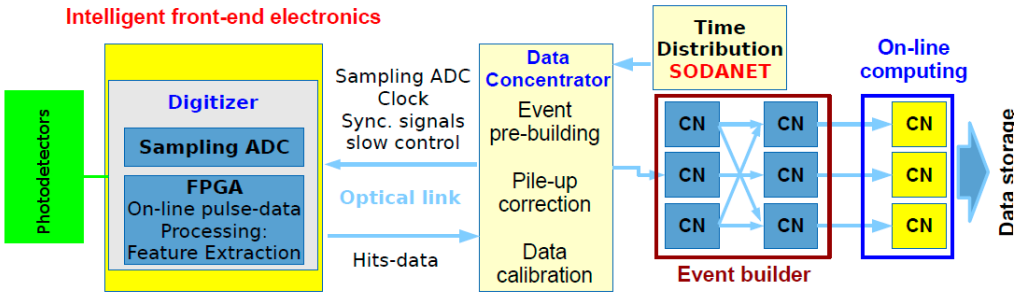
PASTA provides measurement of time and charge of the signal from ***microstrip*** sensors.

PASTA uses 160 MHz clock giving a coarse timestamp with precision of 6.25 ns. Special schematics implemented in the chip provides fine timing with resolution of ≈50 ps.
A charge is measured by the *TOT* method.

For the *pixel* detector of PANDA a trigger-less readout electronics based on ToPiX chip is under development.

Electromagnetic calorimeter

In PANDA the ADC trigger-less chain is under realization, *but on the μTCA platform …*



The trigger-less readout chain of the PANDA Forward Spectrometer.

Feature extraction algorithm which can be embedded in FPGA allows to greatly decrease the volume of data to be transferred. Instead of transmitting all the ADC samples, only time and charge of the hit are delivered to the next stage of the DAQ chain.
This algorithm is under development in different projects (PANDA, COMPASS, …).

!

Straw tracker

I.Konorov developed so-called “iFTDC” which is a TDC module built using FPGA chip.

iFTDC can work both in triggered or trigger-less mode (this has been tested and confirmed), has precision down to 150 ps: well above the requirements of the straw tracker.

It is planned to use iFTDC in COMPASS, NA64 and is reasonable to employ it in SPD.

Straw tracker group is studying also other options for FEE.

iFTDC

Specification

- ARTIX7 FPGA XC7A-35
- 64 channels,
- Programmable signal edge or both edges
- **Bin size : 1 ns, 0.5 ns, 0.25 ns (32 channels)**
- **Time resolution : 300ps, 170 ps, 10 ps**
- **Differential nonlinearity : 10%, 20%, 40%**
- **Trigger less capable data flow**

Applications

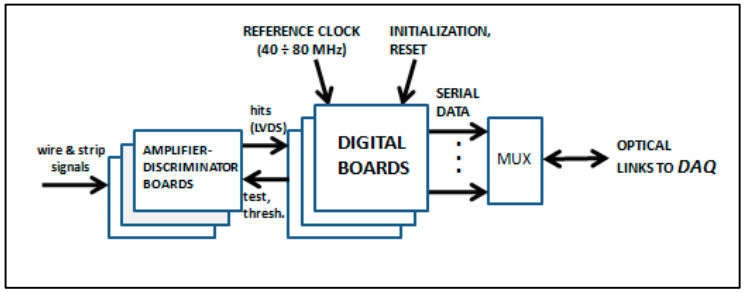
- MWPC(tested), Drift Chambers
- Scintillation Counters with limited requirements for time resolution

Range system

The SPD range system closely follows the design of the range system of PANDA,
which is in a well-advanced state.
Analog front-end electronics is ready (amplifier-discriminator, preamplifier-invertor).

The digital part of the PANDA front-end electronics is in progress.
Its properties are similar to what we want for the SPD-DAQ:

- no trigger: readout by clock signals
- timestamp attached to data
- buffer memory
- use of FPGA chips
- optical links to DAQ



Block diagram of the data stream in PANDA

But digital part is in VME standard!!

Front-end electronics for the free-running DAQ-SPD

What is the status of FEE for the SPD detectors?

None of the SPD detectors has an adequate electronics for the moment.

Nevertheless, in some other experiments there are running developments of the front-end electronics which could be suitable for the DAQ-SPD.

None of these developments has been finalized yet.

Let us look what is available.

Summary for front-end electronics

1. Front-end electronics suitable for free-running DAQ is being created in different new experiments, some of these developments are close to a final stage.

2. Some modifications could be required for use of this electronics in SPD.

3. **The SPD detector groups have to take care of front-end electronics of their detectors capable to run with a trigger-less DAQ.**

Common discussions of the detector and DAQ teams are necessary!