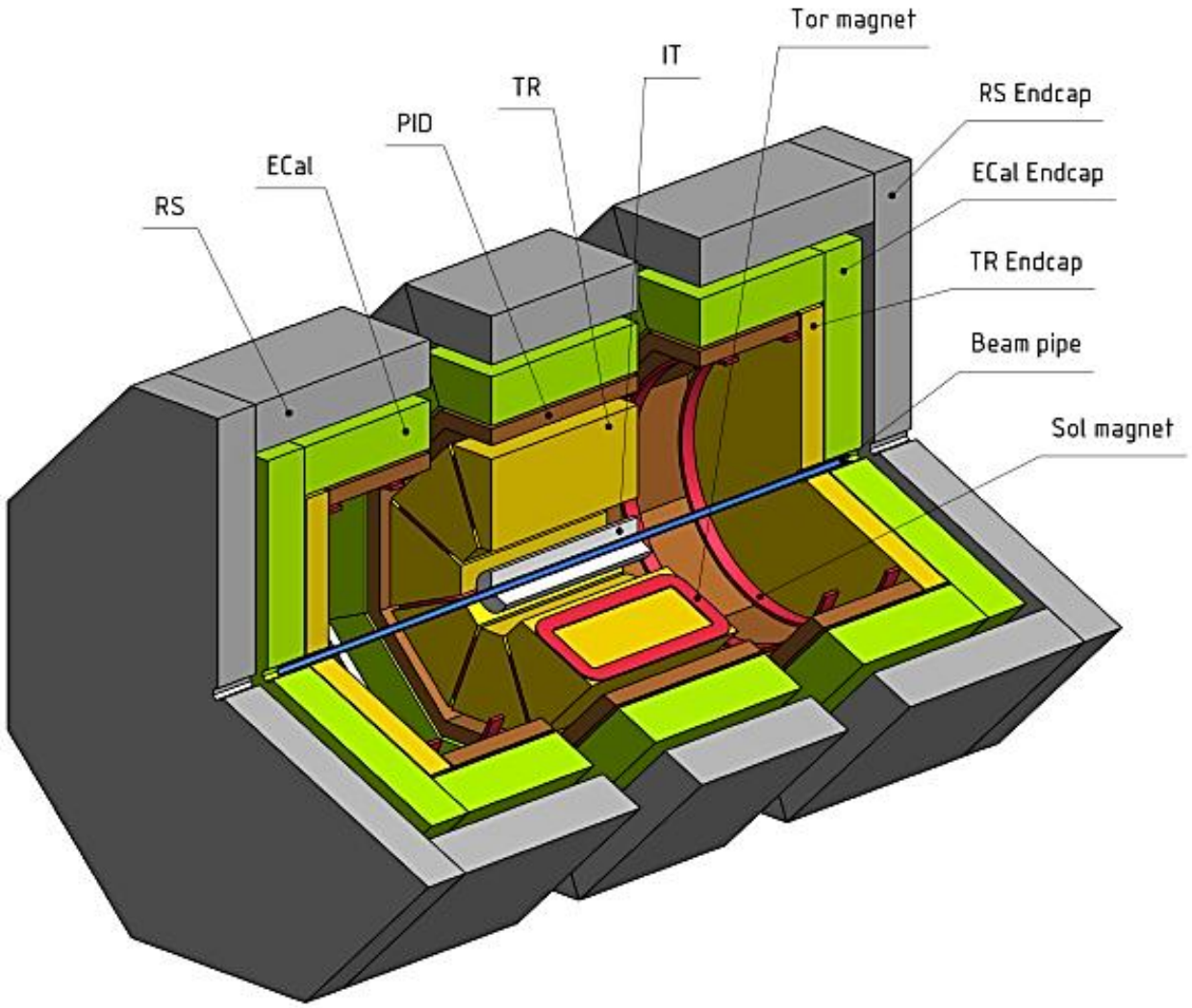
Status and plans for the silicon vertex detector

N. Zamyatin on behalf SPD collaboration

18 March 2019

SPD facility



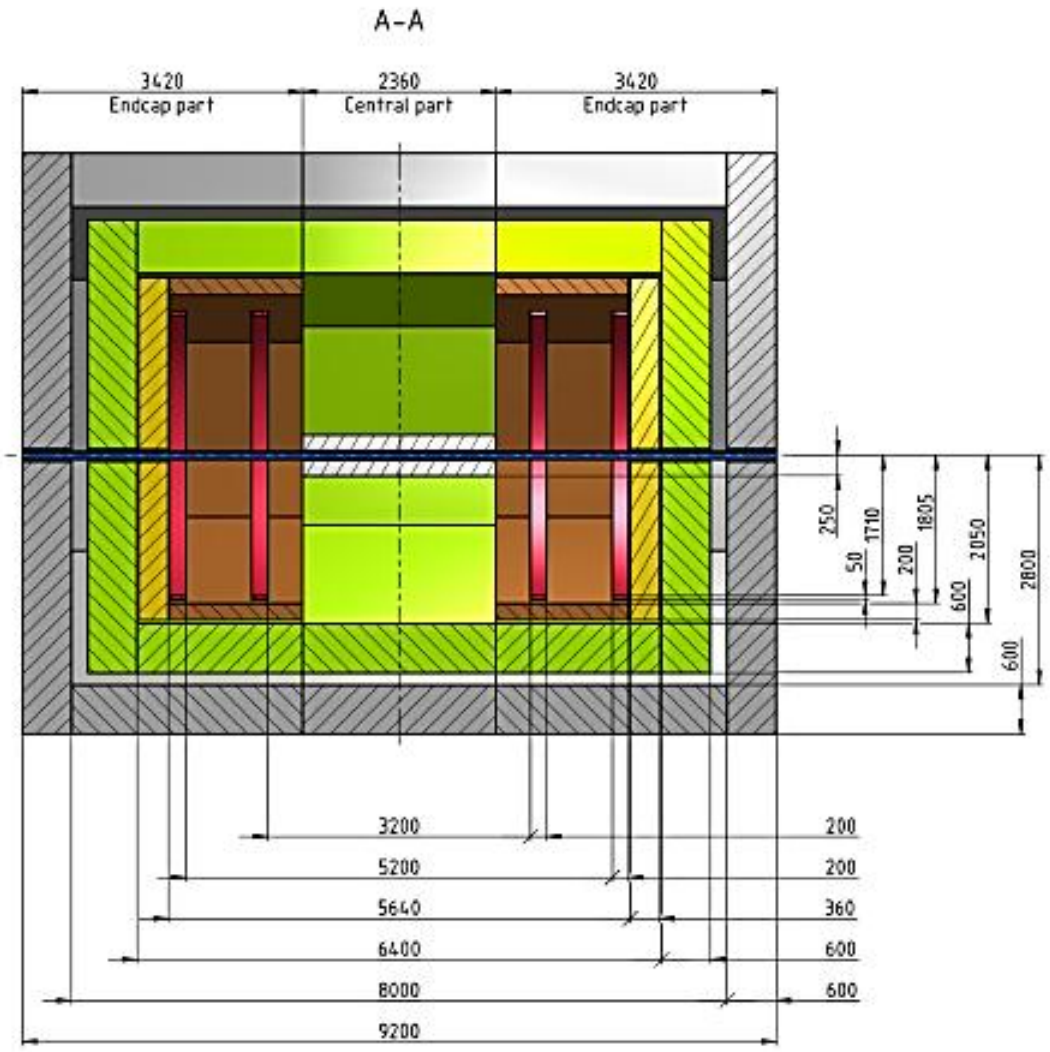


Fig.1 General view (left) and general dimensions (right) of the detector

Inner Tracker Layout

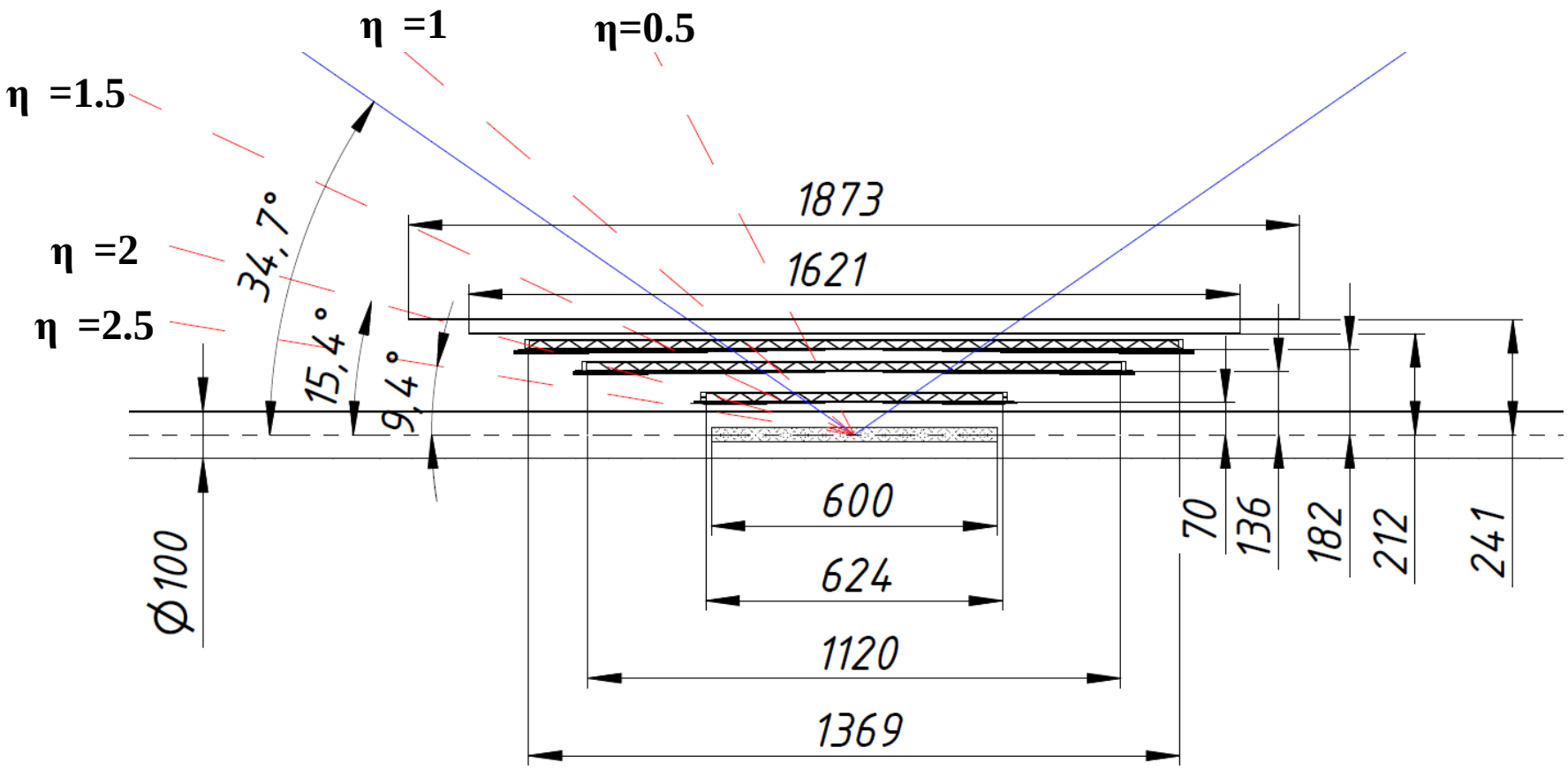


Fig.2 Cross-section of Inner Tracker

Primary goal of IT: determine coordinates of primary and secondary vertexes for rejection of physical background ($\pi^{\pm}$ for DY processes)

Performance requirements of the Inner Tracker

From general conditions:

Number of coordinate layers - 5;

Inner Tracker based on Double Side Silicon Detector (DSSD) thickness 300 μm;

Material budget of 1 layer include:

- Si (300 μm)= $0{,}0032X_0$;
- Kapton cable = $0{,}0016X_0$ (1 cable) ÷ $0{,}096\,X_0$ (6 cables);
- Carbon frame=$0{,}005X_0$;

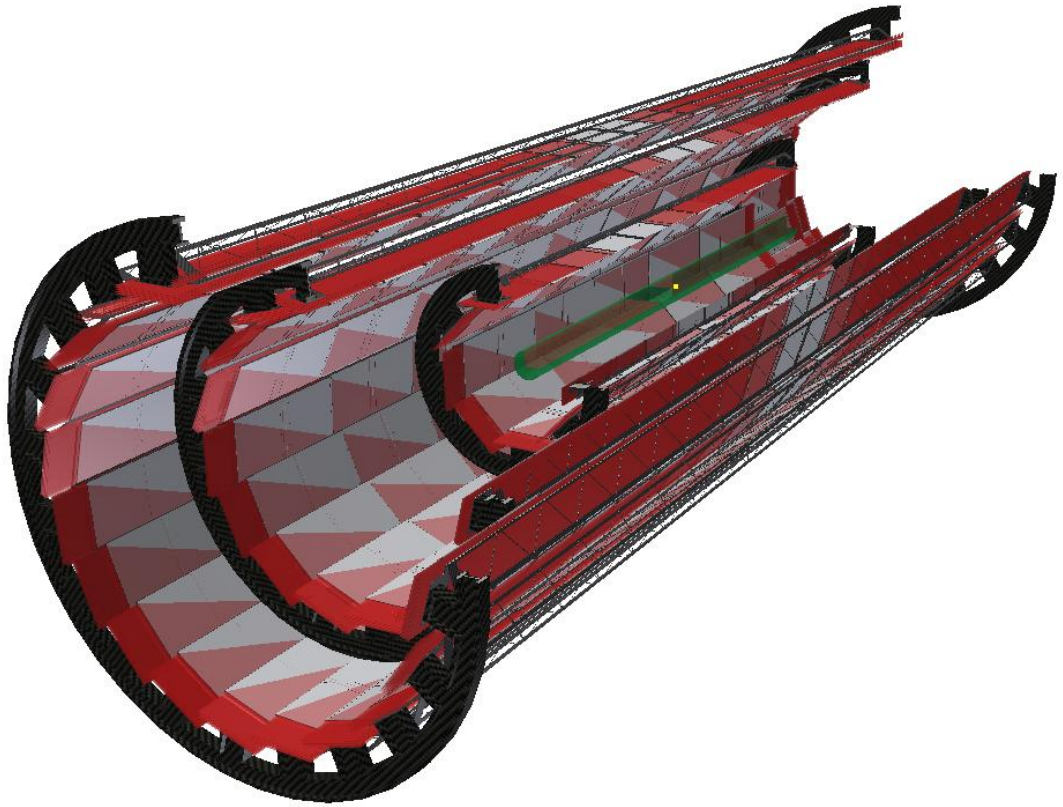
Barrel cover up to $|\eta| = 2$;

End-cap cover up to $|\eta| = 2{,}5$;

Track reconstruction efficiency for muons >99% at $p \leq 13$ GeV/c (for $0 \leq |\eta| \leq 2{,}5$);

Coordinates resolutions: $\sigma_{r\varphi} < 50$ μm, $\sigma_z < 100$ μm.

Inner Tracker Layout



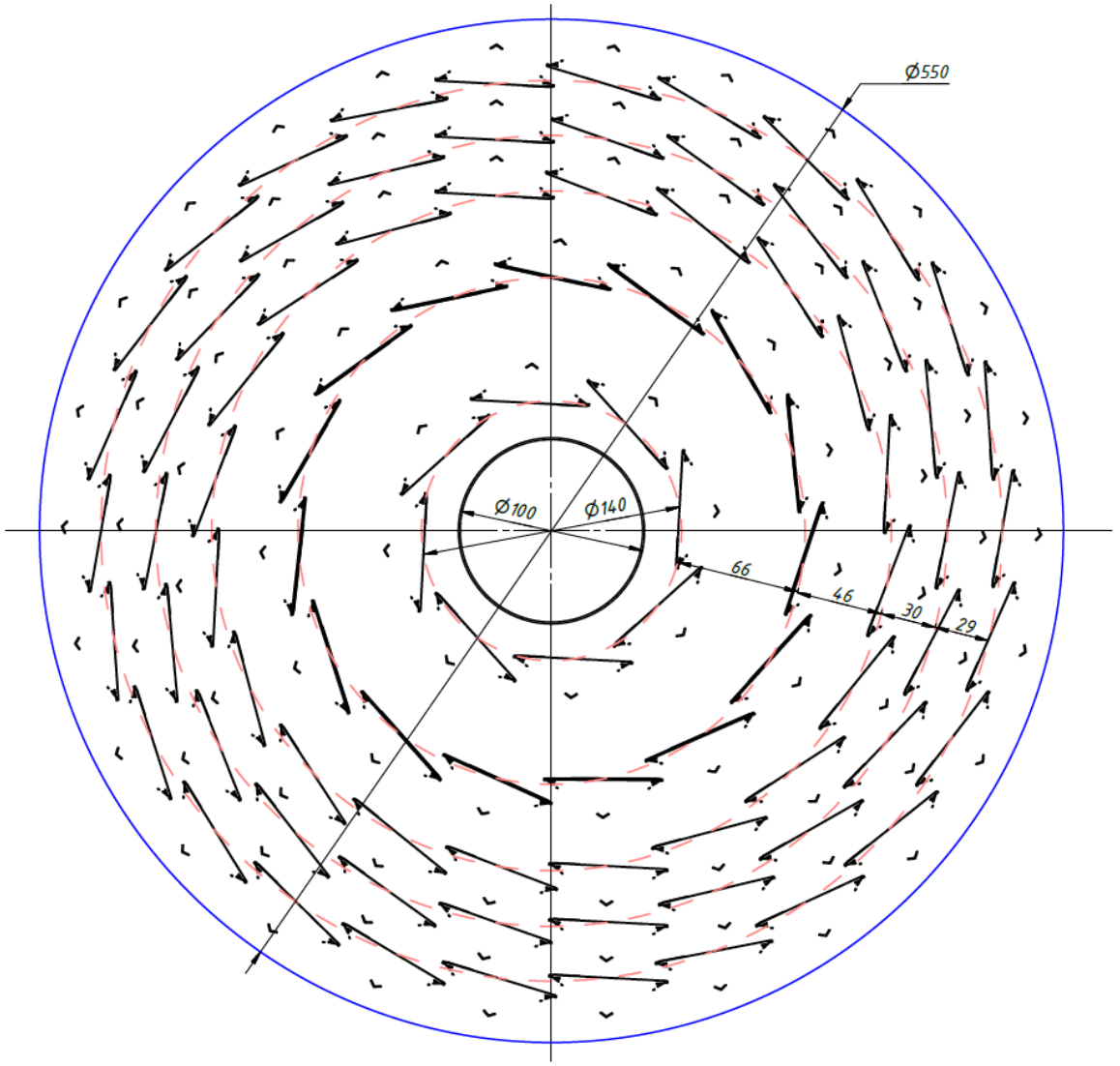


Fig.3 General view of 3 layers IT (left) and $r\varphi$-plane of all IT (right)

Layer parameters

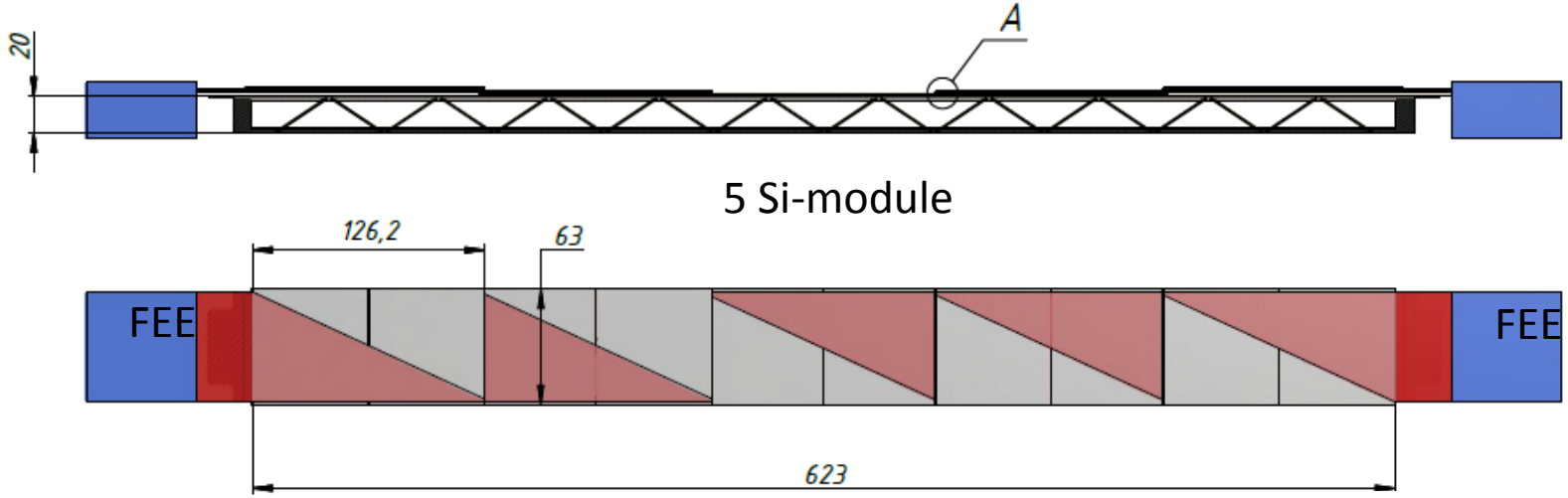
	Number of Si detectors (63x63) on ladder	Number of ladders	Si detectors	Area, m^2	Number of FEE channels (two sensors connected strip to strip)
1 layer	10	8	10 8=80	0,3	(80:2)x640x2=51 200
2 layer	18	15	18 15=270	1	(270:2)x640x2=172 800
3 layer	22	20	22 20 2=440	1,7	(440:2)x640x2=281 600
4 layer	26	22	26 22 2=572	2,3	(572:2)x640x2=366 080
5 layer	30	26	30 26 2=780	3	(780:2)x640x2=499 200
			Total = 2142	Total = 8,5	Total= 1 370 880

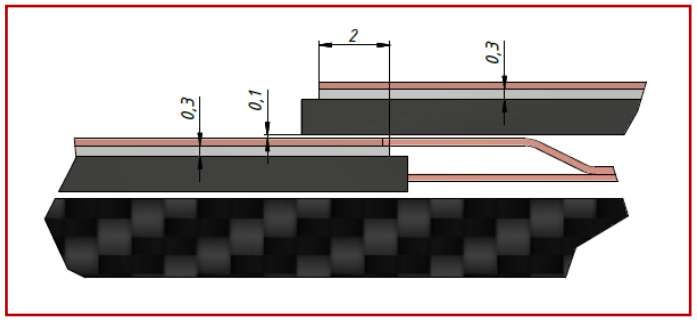
Comments:

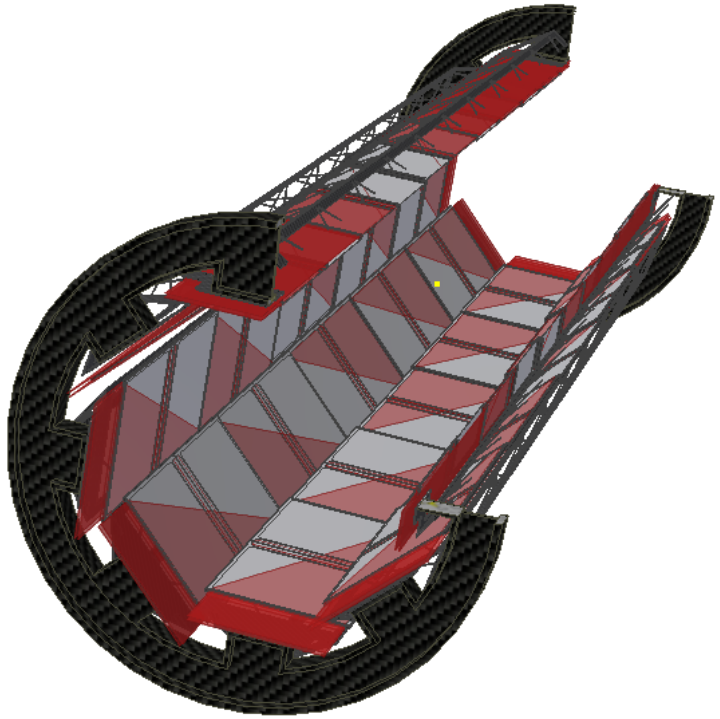
Total numbers of FE chips = 10710

Total power FEE chips~2mW/ch. $1,4*10^6$ = 2,8 kW

View of 1st Barrel Layer







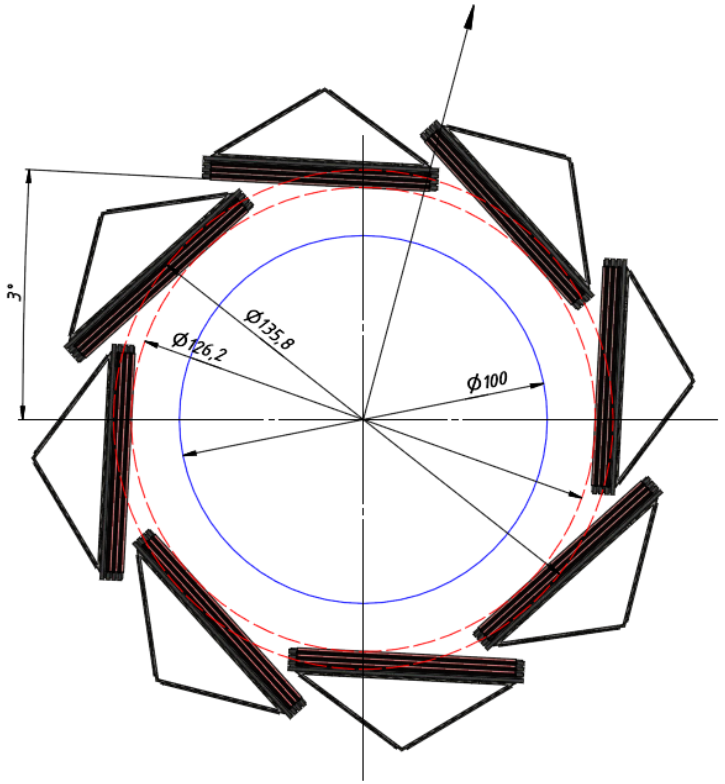
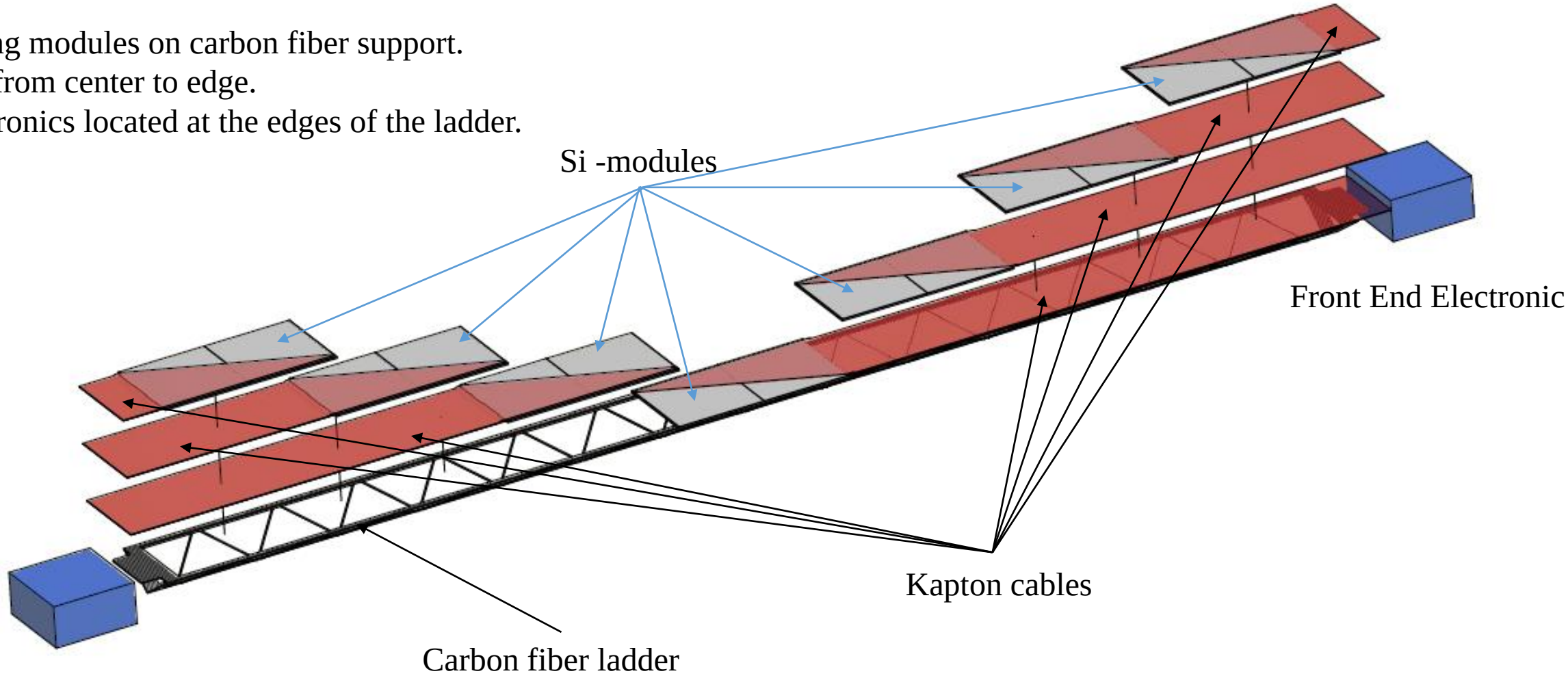


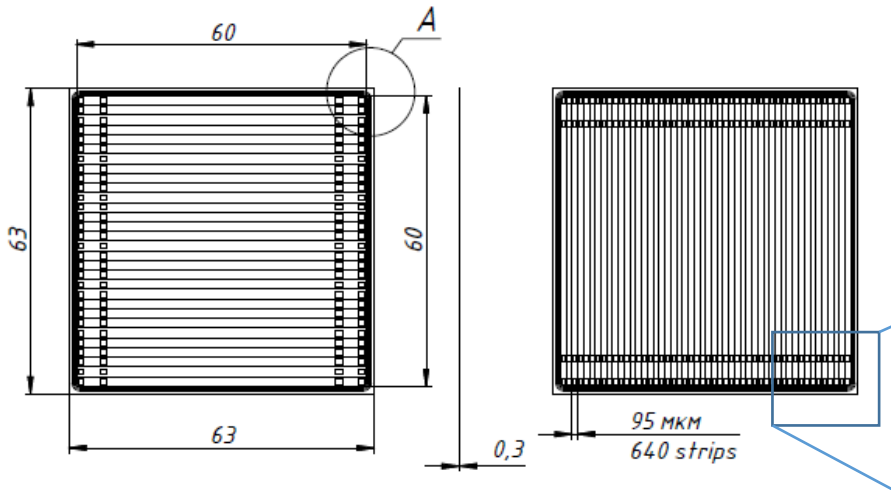
Fig.4 *Upper*: Schematic view of first barrel layer ladder;
Bottom: General view (left) and $r\varphi$-plane (right) of first barrel layer

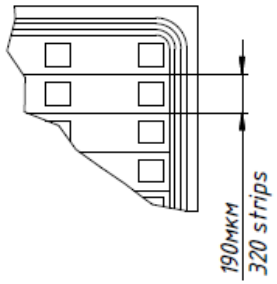
View of carbon fiber ladder with Si-modules

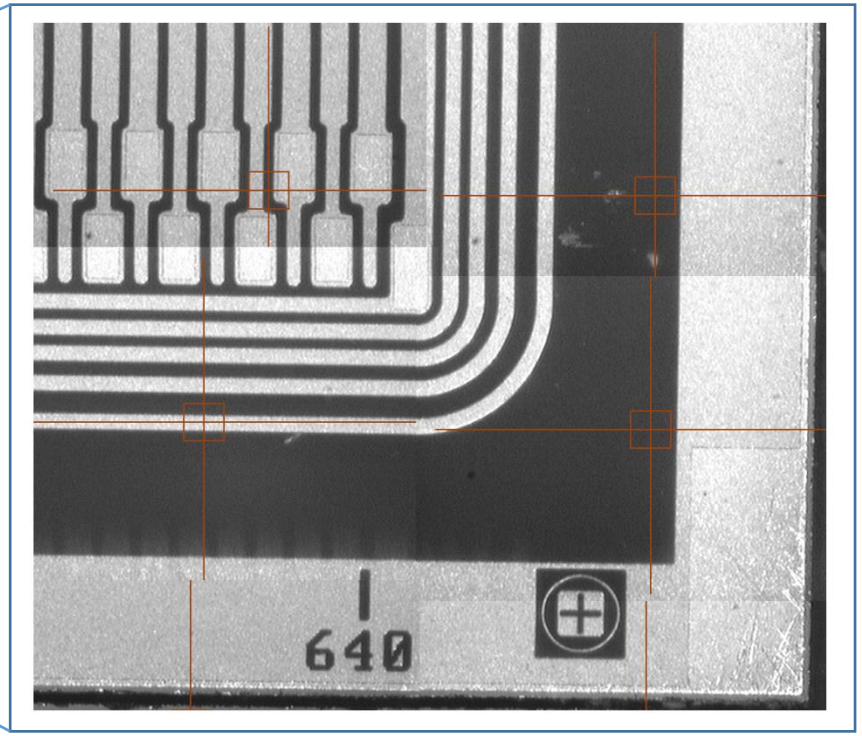
Laying modules on carbon fiber support.
Puts from center to edge.
Electronics located at the edges of the ladder.



Detector’s topology

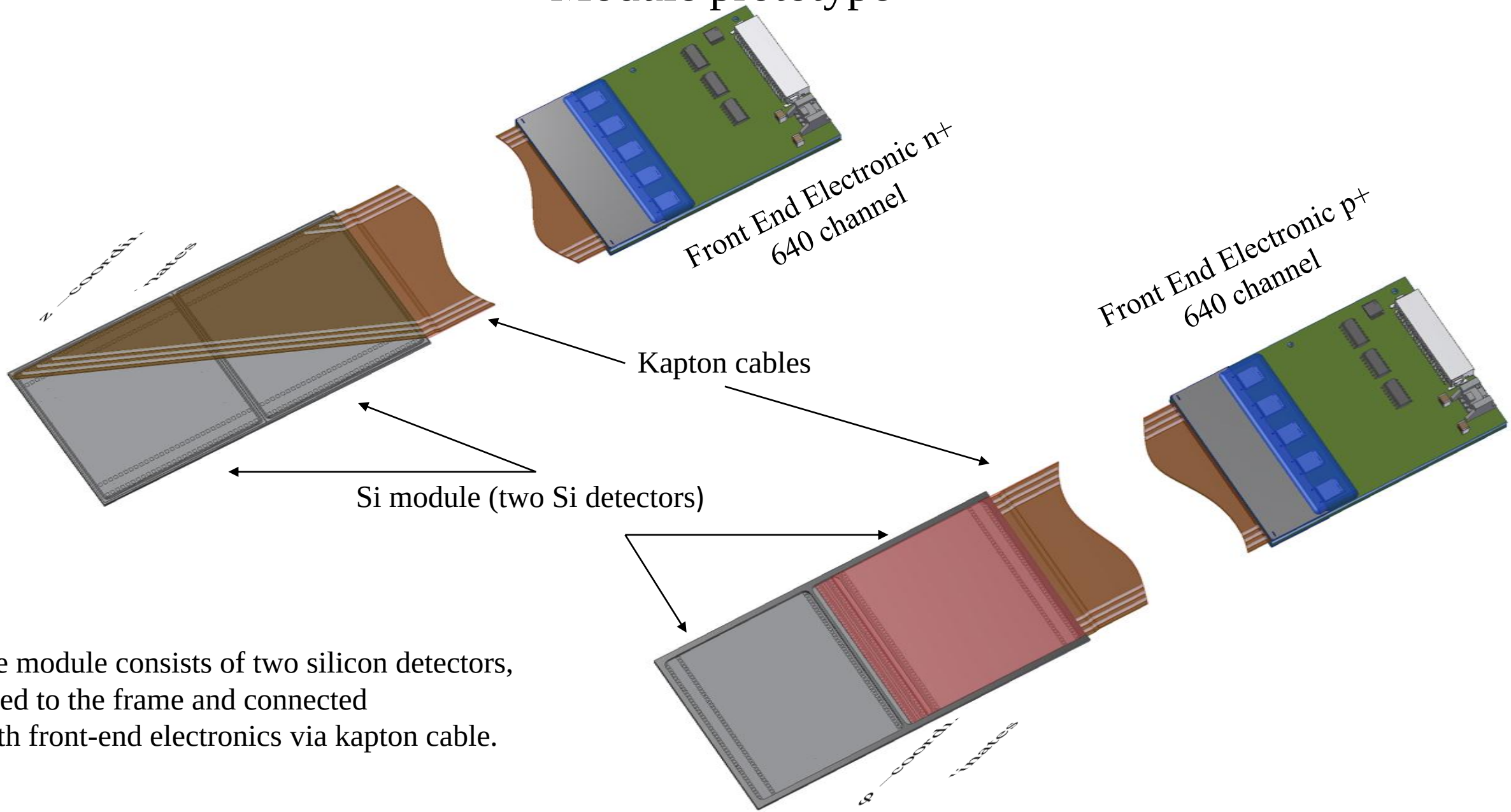






- Size: 63x63x0,3 mm^3 (on 4” – FZ-Si wafers)
- Topology: double side microstrip (DSSD) (DC or AC coupling)
- Pitch p^+ strips: 95 μm;
- Pitch n^+ strips 190 μm;
- Stereo angle between p^+/n^+ strips: 90^0
- Number of strips: 640 (p^+)×320(n^+)

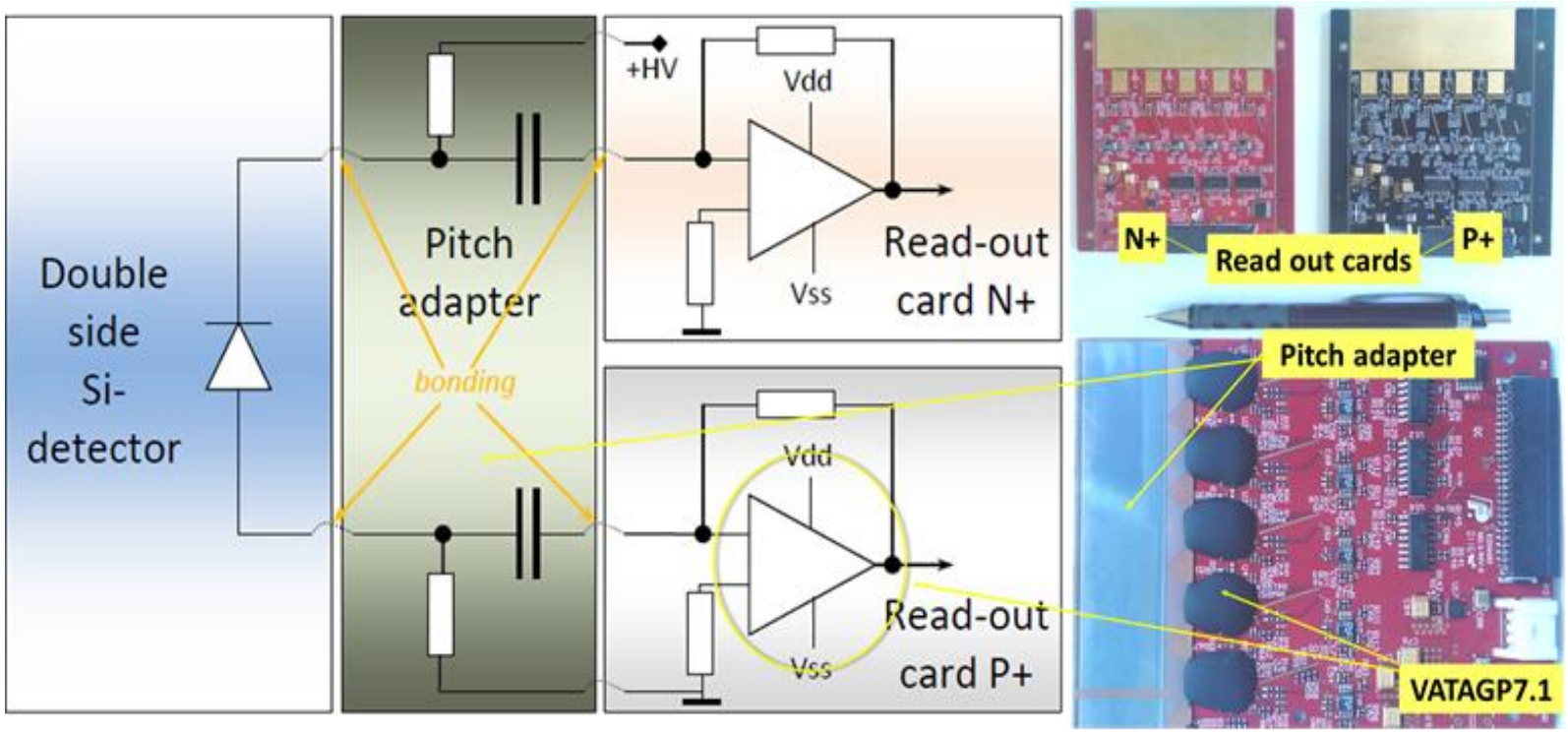
Module prototype



The module consists of two silicon detectors,
glued to the frame and connected
With front-end electronics via kapton cable.

The functional scheme of detector module and appearance of two electronic boards

(FE-design of BM@N experiment)



DSSD with DC topology don't contain integral resistors and capacitors (RC), therefore external R, C are required to supply bias voltage to each strip and to electrically decouple the DC current from the electronic inputs. This role is performed by Pitch Adapter (PA) with a topology of two types for p+ and n+ sides of the detector. In addition, PA has topology of contact pads similar to chips located on the side of electronic chips. PA modules are made on sapphire plates with an epitaxial layer of silicon (SOI). Integrated poly silicon bias resistors have a value of 0.7 – 1.0 MΩ, decoupled capacitors have a value of 140 pF. PA is assembled together with read-out ASICs on the read-out card. Positive polarity signals come from detectors to P+ read-out card (black PCB) while negative signals come to N+ read-out card (red PCB).

Parameters of new read-out chip

Readout ASIC VATAGP7.3.

Number of sensitive pre-amplifier (CSA) inputs - 128

Input charges (dynamic range) - -30fC +30fC

Peaking time (slow shaper) - 500ns (typ.)

Peaking time (fast shaper) - 50ns

Noise (ENC)- 70e +12e/pF (typ.)

Lowest threshold (no capacitance) 0.12fC

Good linearity for charges up to +/- 15fC

Gain from input to output buffer (diff. output currents) 16.5μA/fC

Output Serial analog multiplexer with 20MHz clock speed nominal.

Voltage supply - +1.5V, -2.0V

Power dissipation per channel – tbd

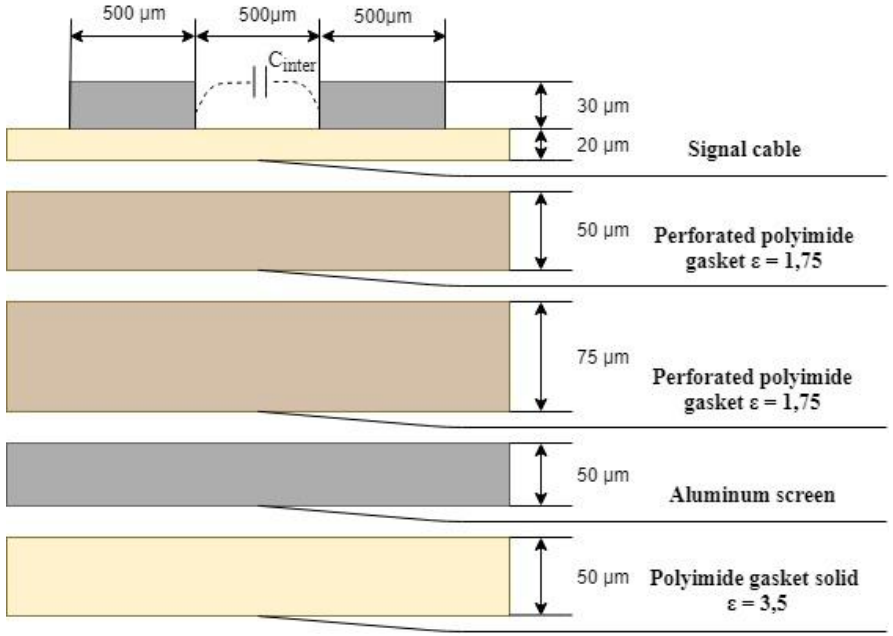
We are waiting delivery of first 10 ASICs at the end of Q2 2019

Polyimide cable

Manufacturing: Light Technologies Ukraine. Ukraine, Kharkov

viatcheslav.borshchov@cern.ch, maksym.protsenko@cern.ch

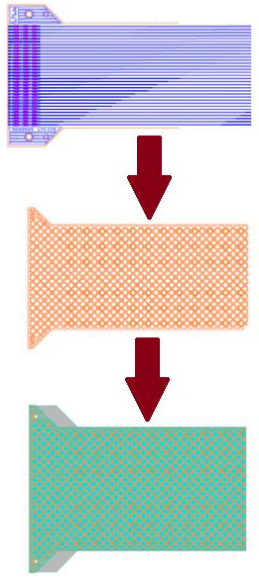
Maximum cable length 600 mm



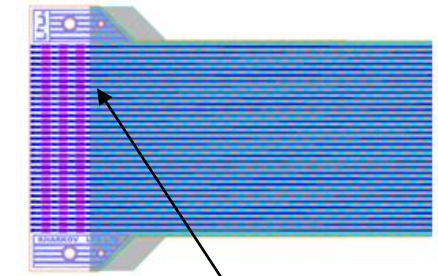
Signal cable

Perforated dielectric strip (perforation area 70%)

Shielding layer with gasket



The combination of signal and shielding layers

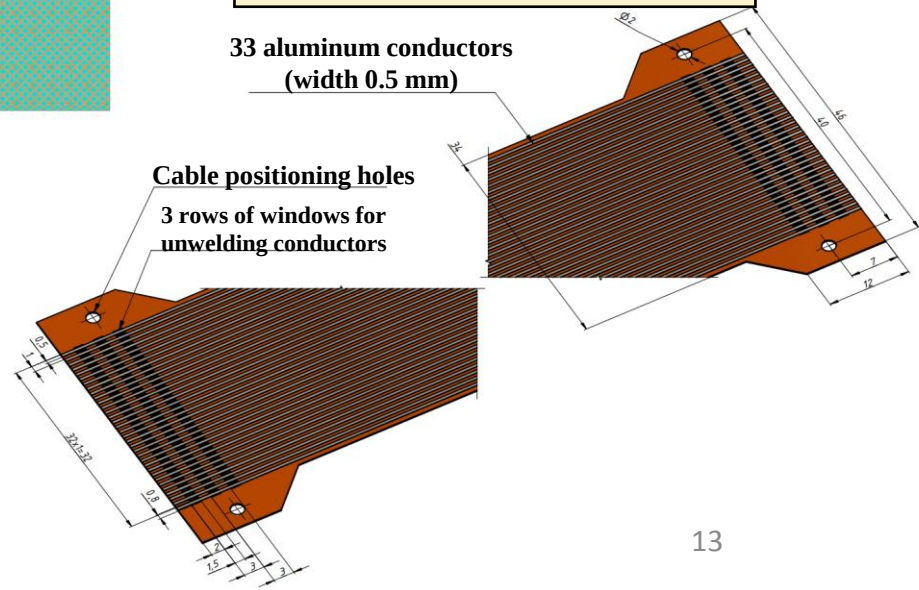


Additional holes for combining layers

33 aluminum conductors (width 0.5 mm)

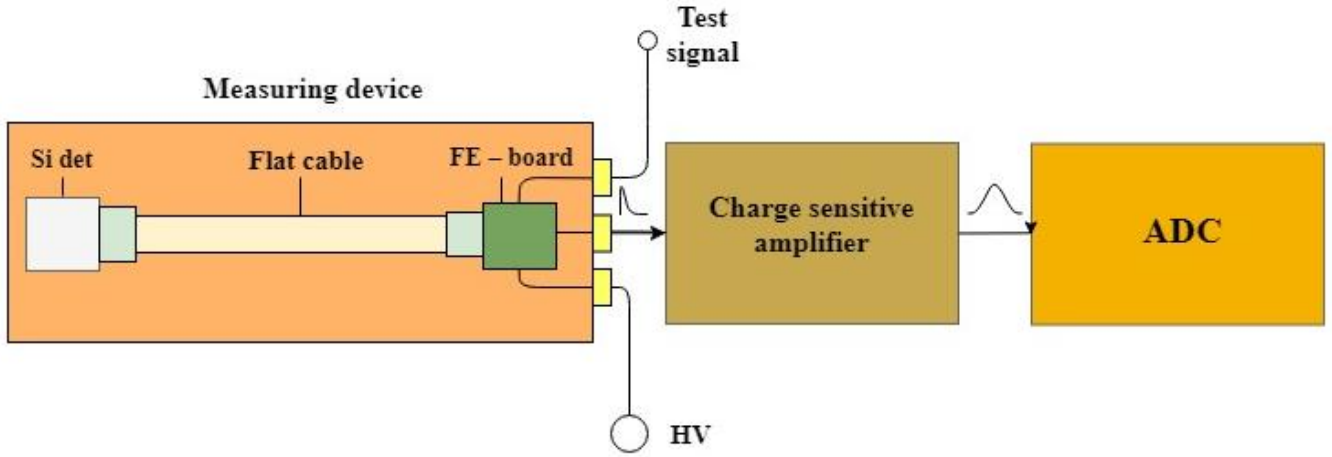
Cable positioning holes

3 rows of windows for unwelding conductors



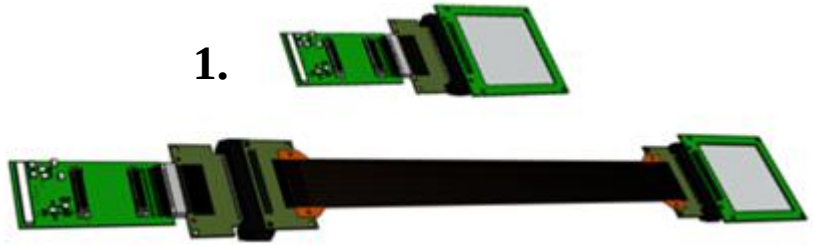
Resistance of one conductor (**1200**):	0,96 Ω
Specific resistance:	$0{,}8\ \frac{\text{мΩ}}{\blacksquare}$
Electrical capacitance between conductors:	16 2 pF

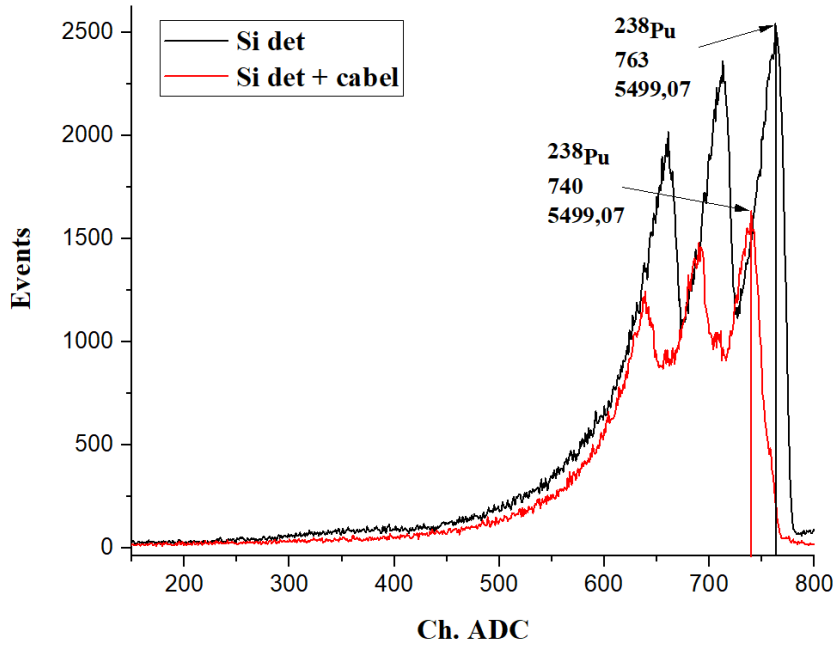
Measurement of the attenuation of α-signal in a polyimide cable without vacuum



1.

2.





Measurements	HV, V	Center ^{238}Pu, ch.ADC	Δ, ch. ADC	$\frac{\Delta}{763}$, %
1. FE – board + Si det (32 p^+ strips)	60	763	23	3,01
2. FE– board + polyimide cable + Si det (32 p^+ strips)	60	740		

The signal attenuation with polyimide cable (600 mm lenght or 1200) is 3%

Plans on 2019

- Design and assembly first prototype of detector module 63x126 mm^2 and 1280 read-out channels;
- Design and optimize kapton cables topology with maximum length (600 mm);
- Preparation of CDR for Inner Tracker part.