# Architecture and Performance of COMPASS DAQ,

## future plans and possibility to adapt the system to other experiments

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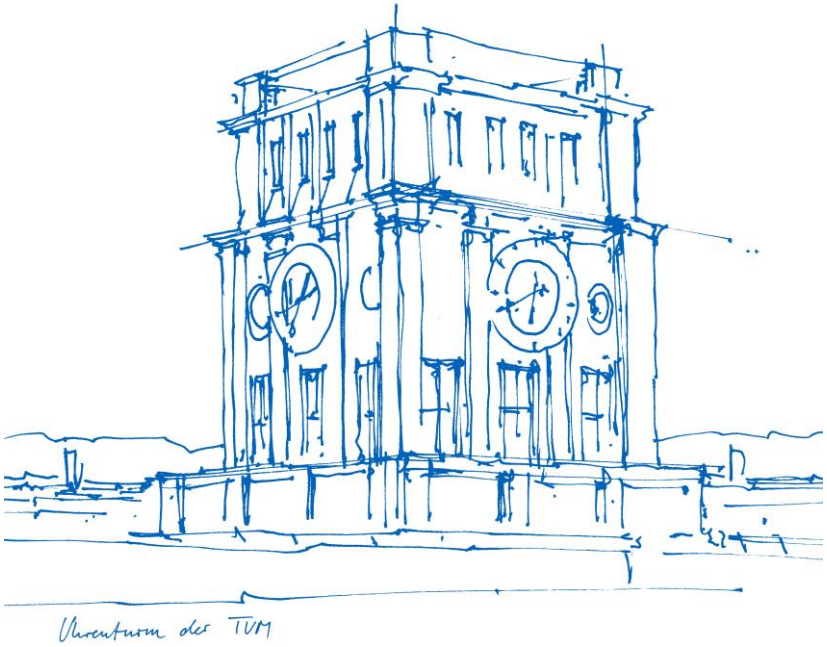
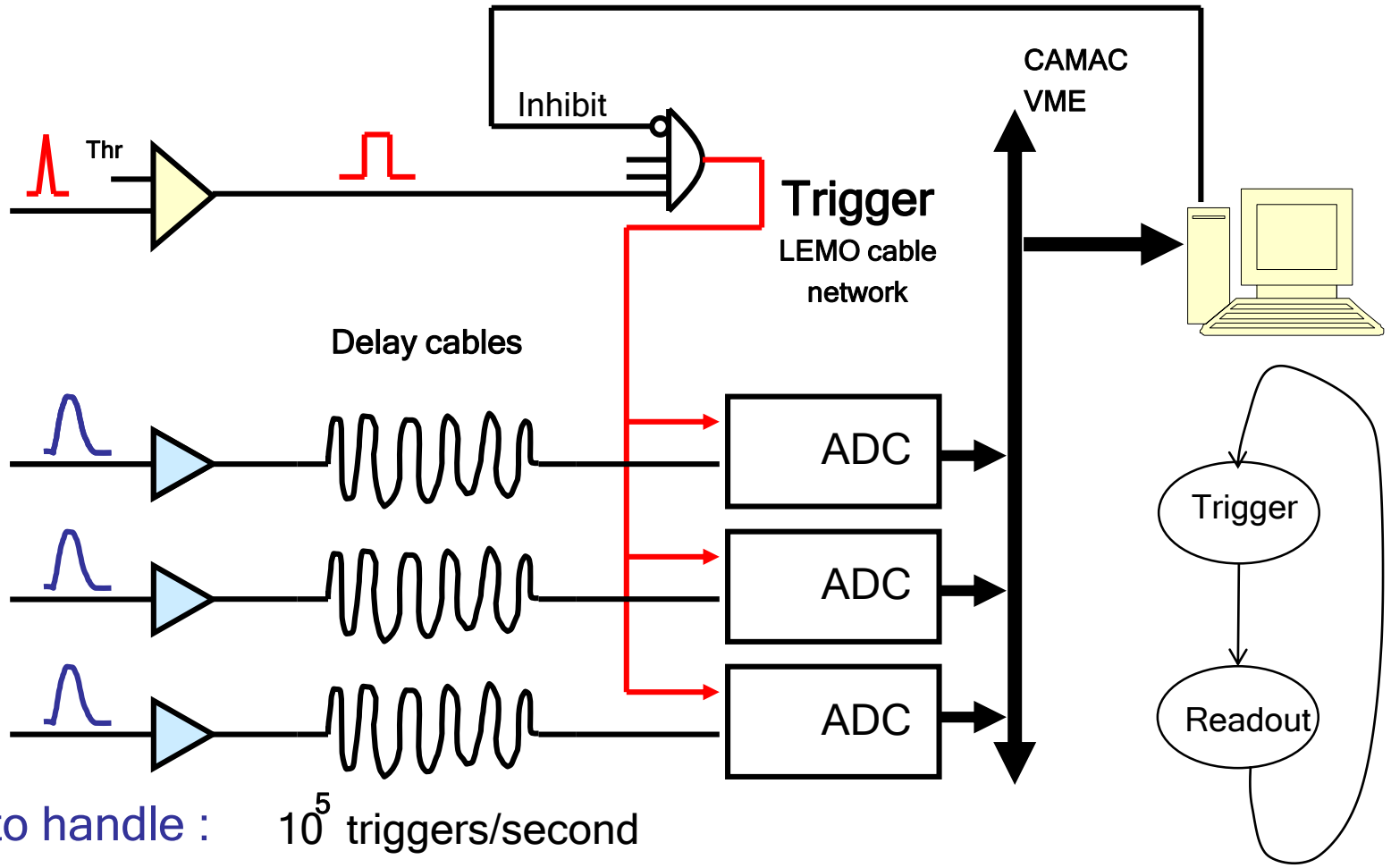
Dubna January 15-th



# Short Introduction

# Classical triggered DAQ



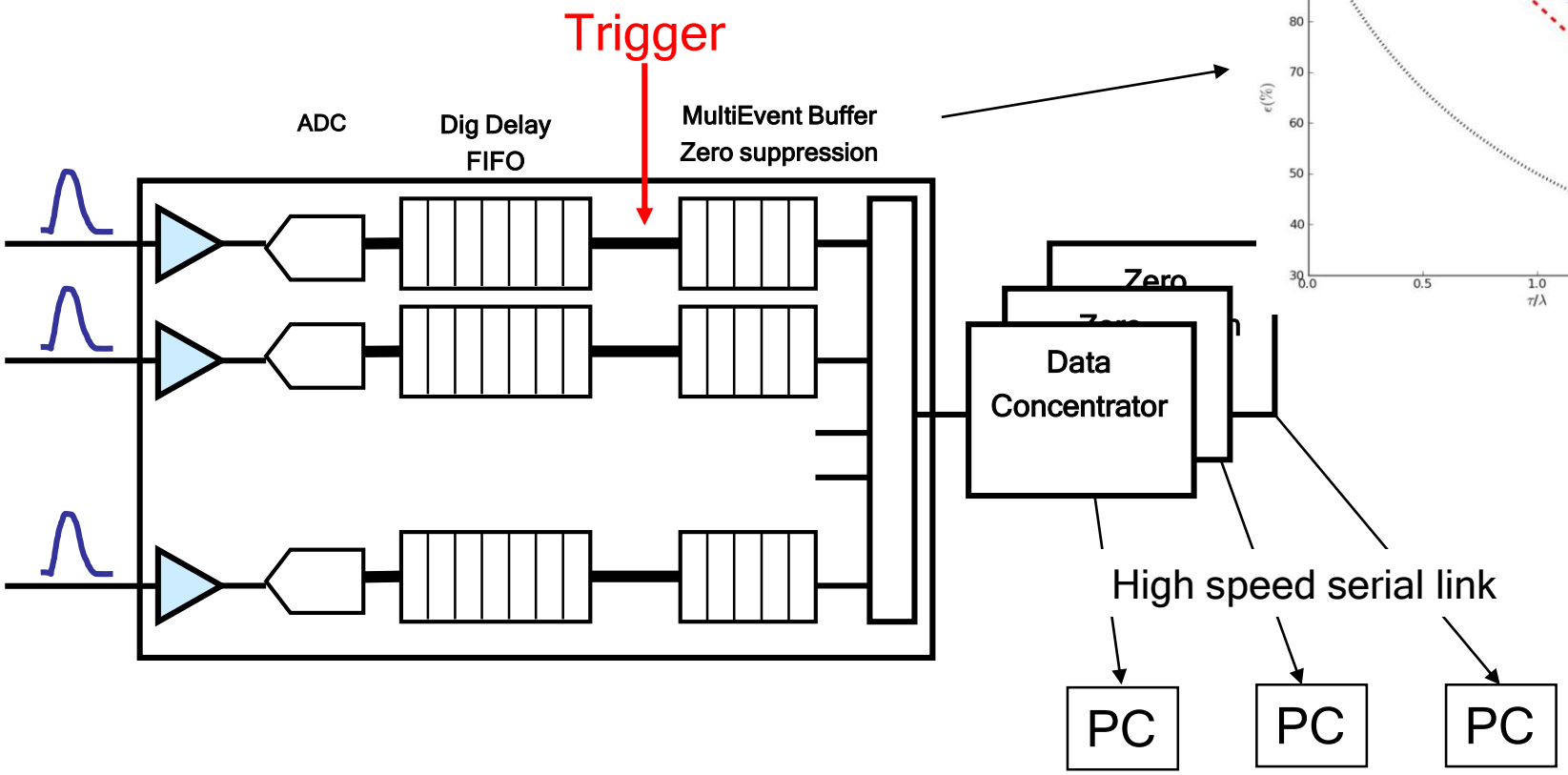

How to handle : $10^5$ triggers/second

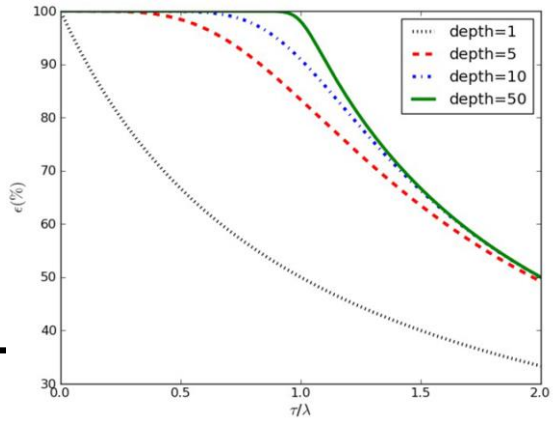
> $10^5$ detector channels

GByte/s data

# Pipeline Front-End

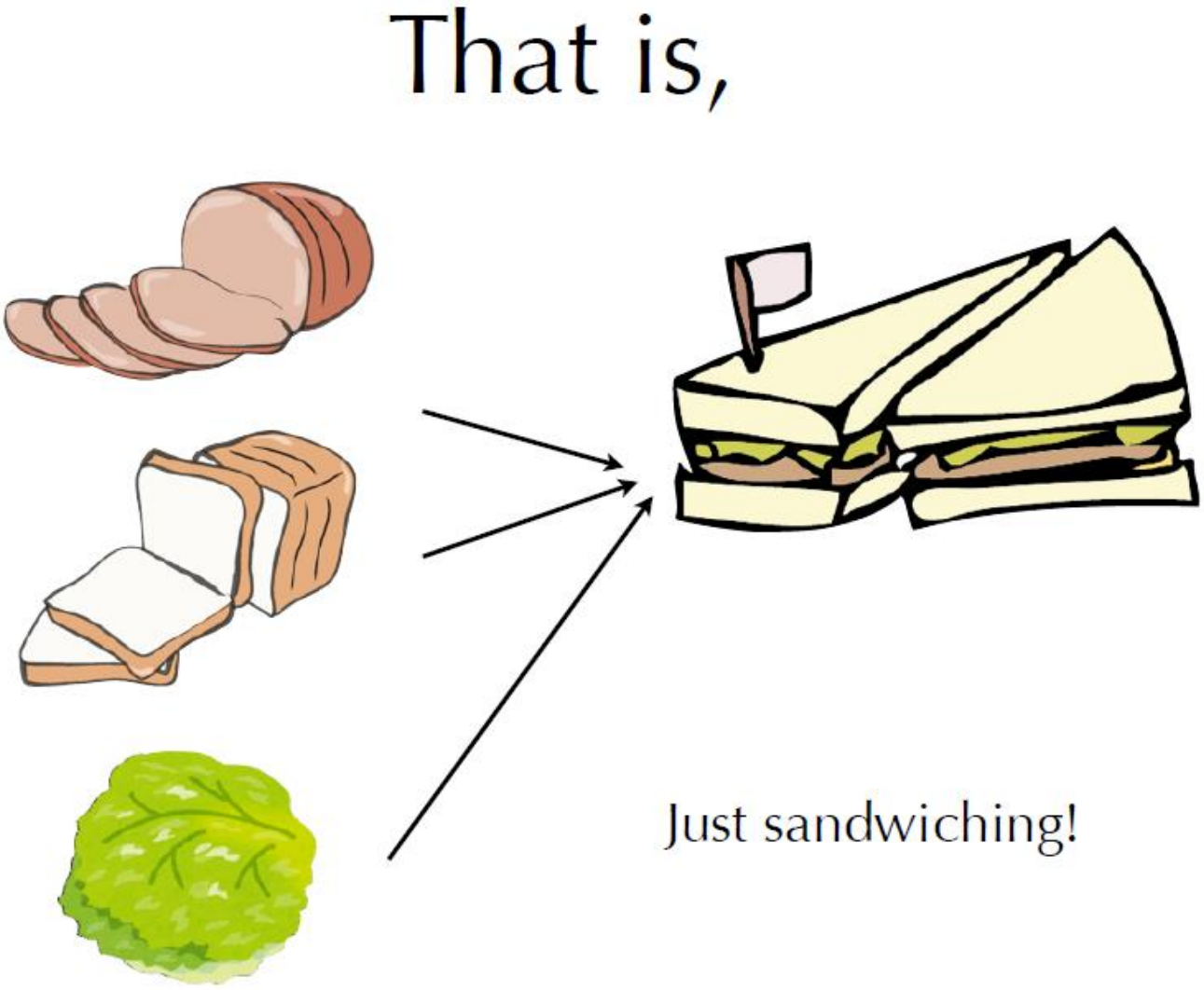
1. Trigger -> Copy data to Multi Event Buffer with speed 40-120 MB/s/ch => 20 TB/s
2. Multi Event Buffer or derandomization => average Trigger rate 30kHz => reduction 1000
3. Zero suppression => reduction 20 => 1GB/s => …




Event Building ?

# What is Event Building

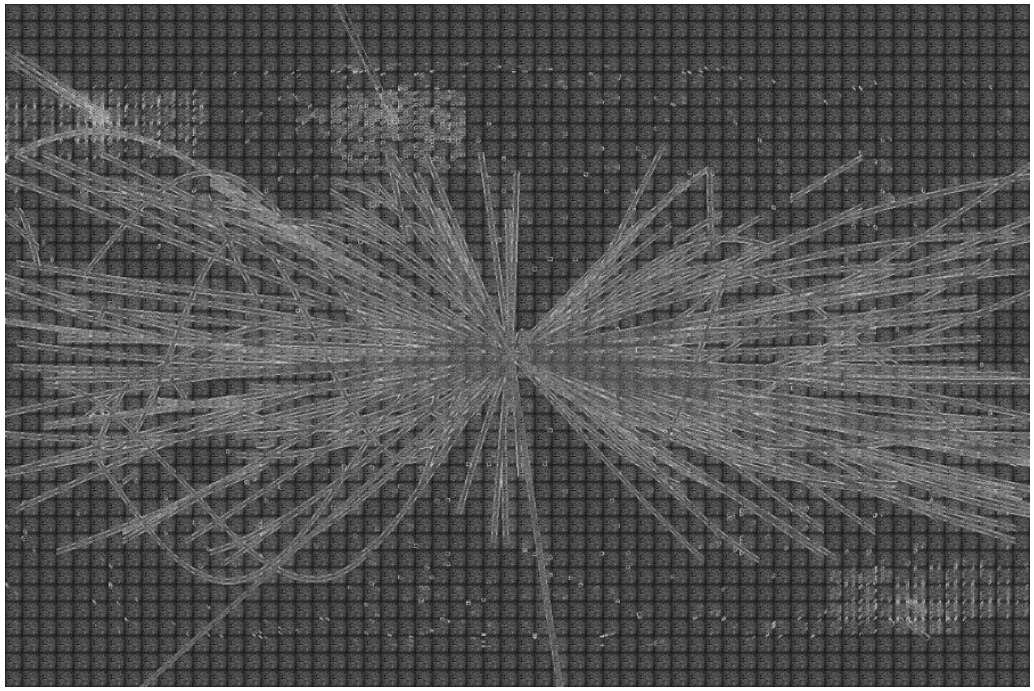


# Event builder => recover Mosaic Image

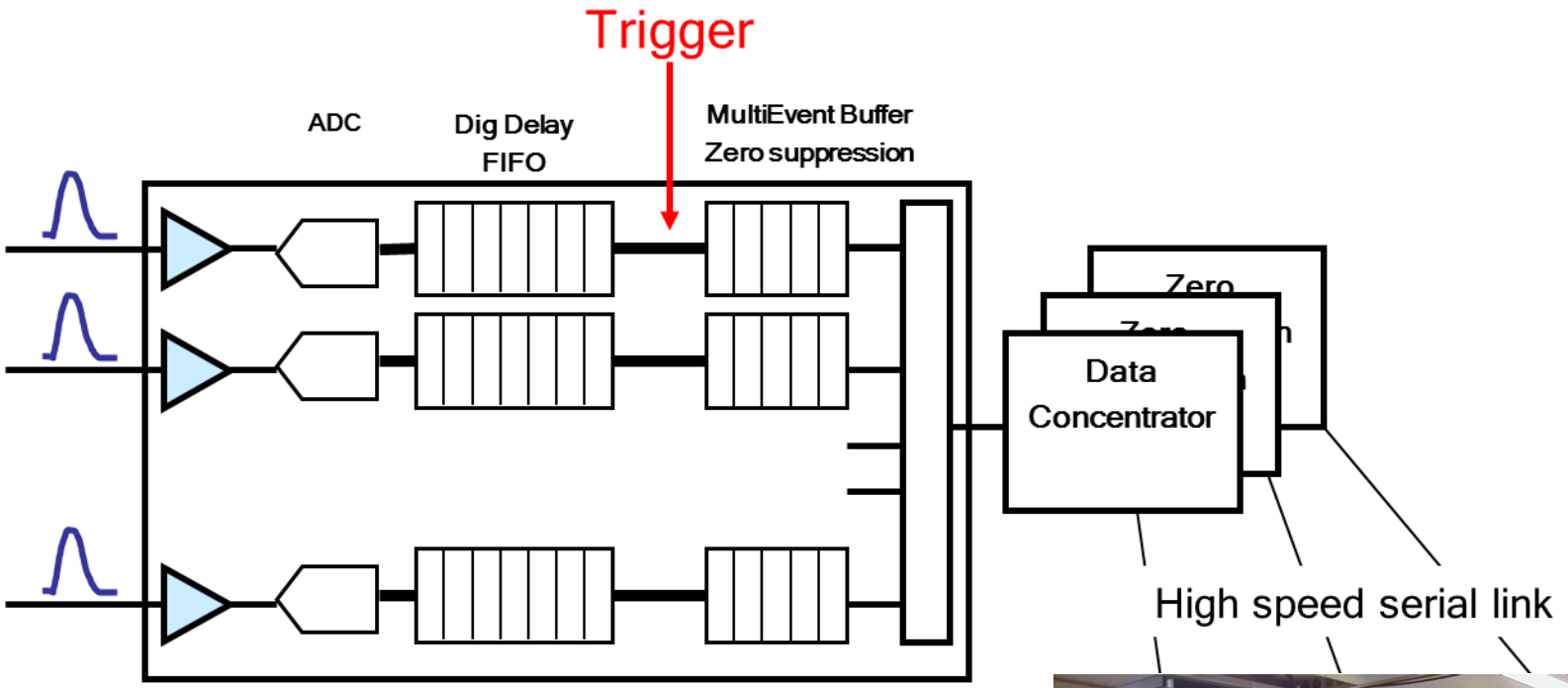
Front-end

Event Builder

Higgs event



# Event Building




Event Build

# COMPASS Experiment

# COMPASS

## Micro pattern detectors

- Silicon Detectors
- GEM, PGEM, PMM

## Scintillating Detectors

- SciFi, BMS, Hodoscopes, CAMERA

## Wire Chambers

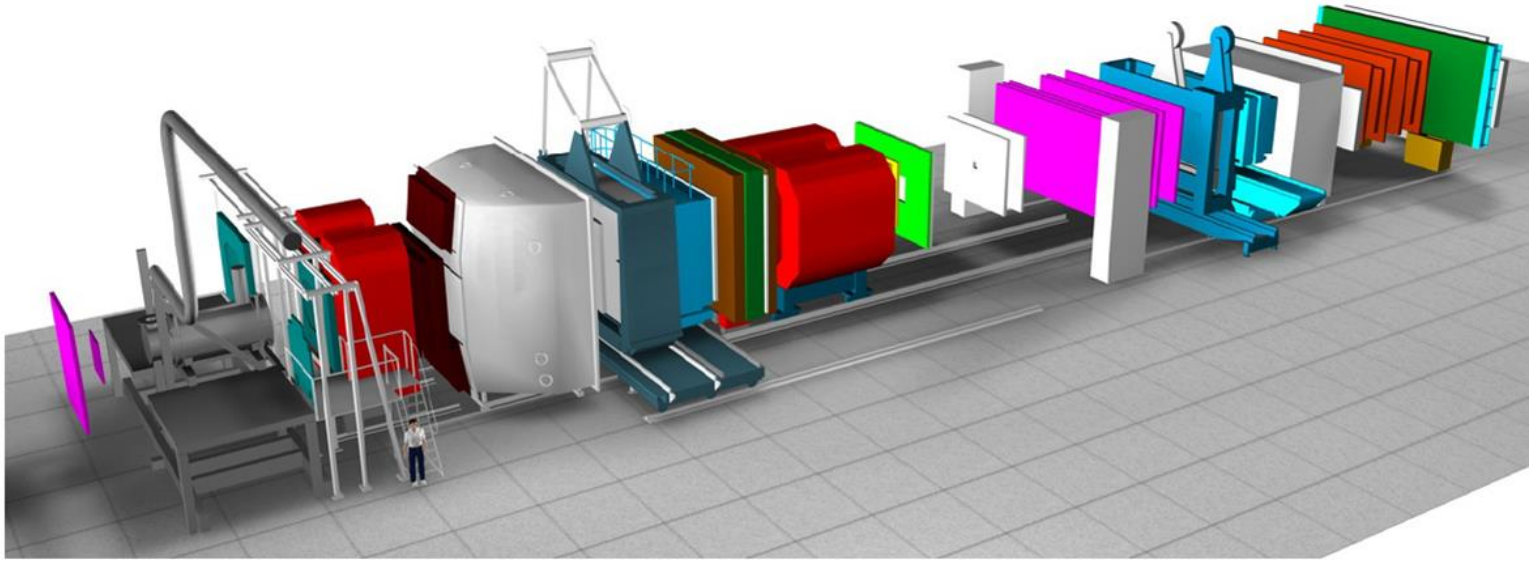
- DC, Straw, W45
- MWPC, RW, MW1, MW2
- DC05

## Calorimeters

- HCAL1,2
- ECAL 0,1,2

## RICH

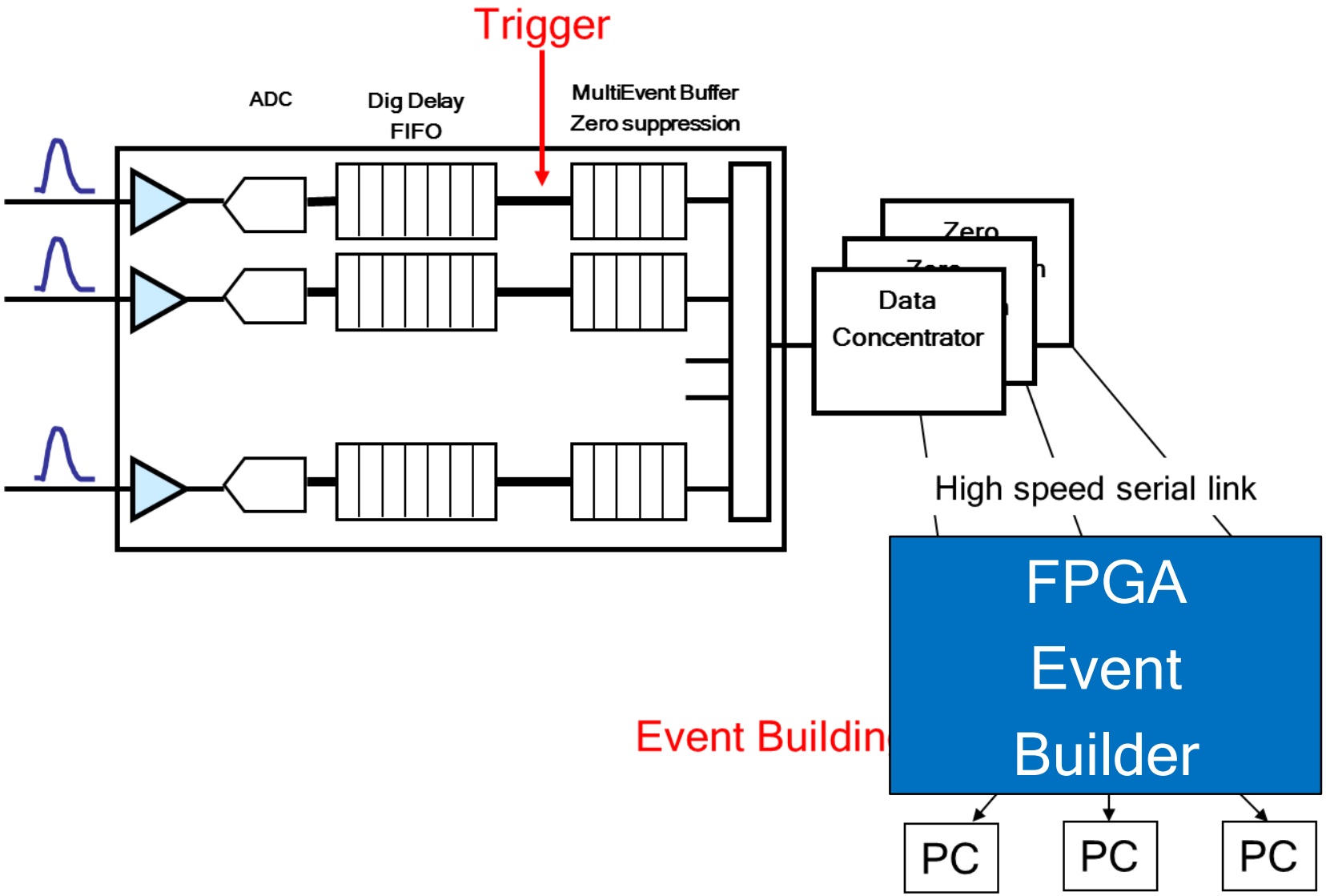
- MAPMT
- MWPC, THGEM



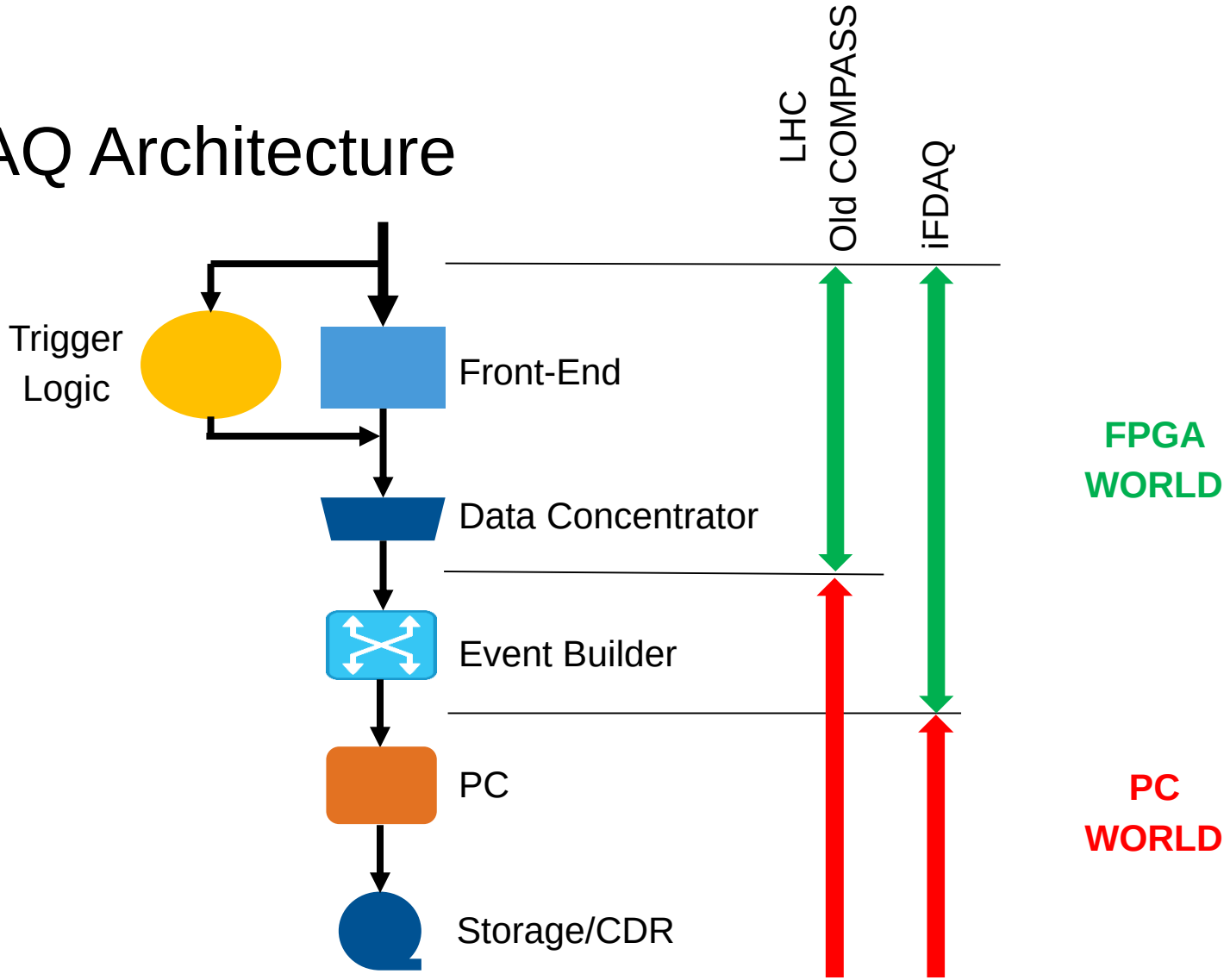
# COMPASS DAQ

- 300k detector channels
- ~2 k FE cards
- 100 Data Concentrators transmit data via optical HOLA Slink interface
  - GESICA
  - HGESICA
  - CATCH
  - SlinkMX
- Trigger Control System (TCS) – distributes TRIGGERS, EVENT HEADERS
- Up to 40 kHz trigger rate capability
- 1.5 GB/s data rate within spill => up to 500MB/s sustained

# Event Building



# DAQ Architecture



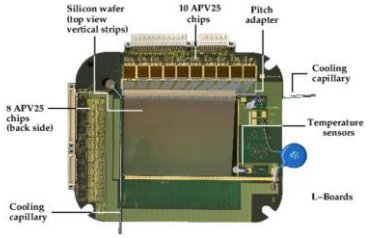
# FRONT-ENDS

# Front-End and DAQ Electronics

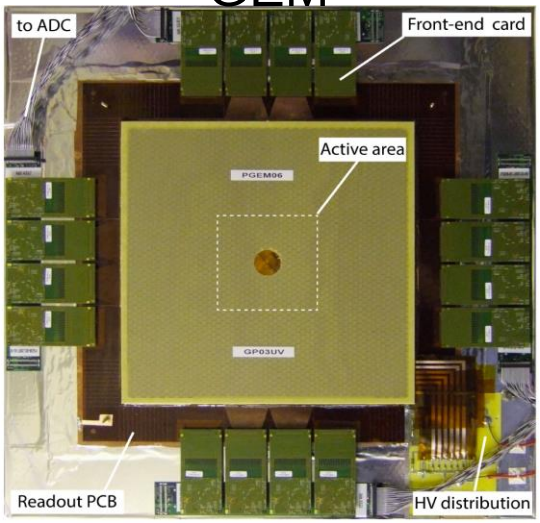
| Detector type | # of channels | Read out electronics | Location |
|---|---|---|---|
| Calorimeters ECAL0, ECAL2 | 4.800 | 12b ADC@80MHz | VME Crate |
| Calorimeters HCALs, ECAL1 | 2.200 | 10b ADC@80MHz | VME Crate |
| Silicon, GEM, PGEM, PMM | ~100.000 | APV25 ASIC | Detector |
| RICH, MWPC | 60.000 | APV25 ASIC | Detector |
| RICH, MAPMT | 12.000 | F1 TDC | Detector |
| SciFi | ~2.600<br>? | F1 TDC<br>GANDALF(FPGA)TDC | VME Crate |
| Beam Momentum Station | 640 | F1 TDC | VME Crate |
| Hodoscopes, VETO | 500 | F1 TDC | VME Crate |
| Wire Chambers | ~60.000 | F1+FPGA TDC | Detector |
| Recoil Detector | 96 | 14b ADC@0.5(1.0)GHz<br>GANDALF | VXI Crate |

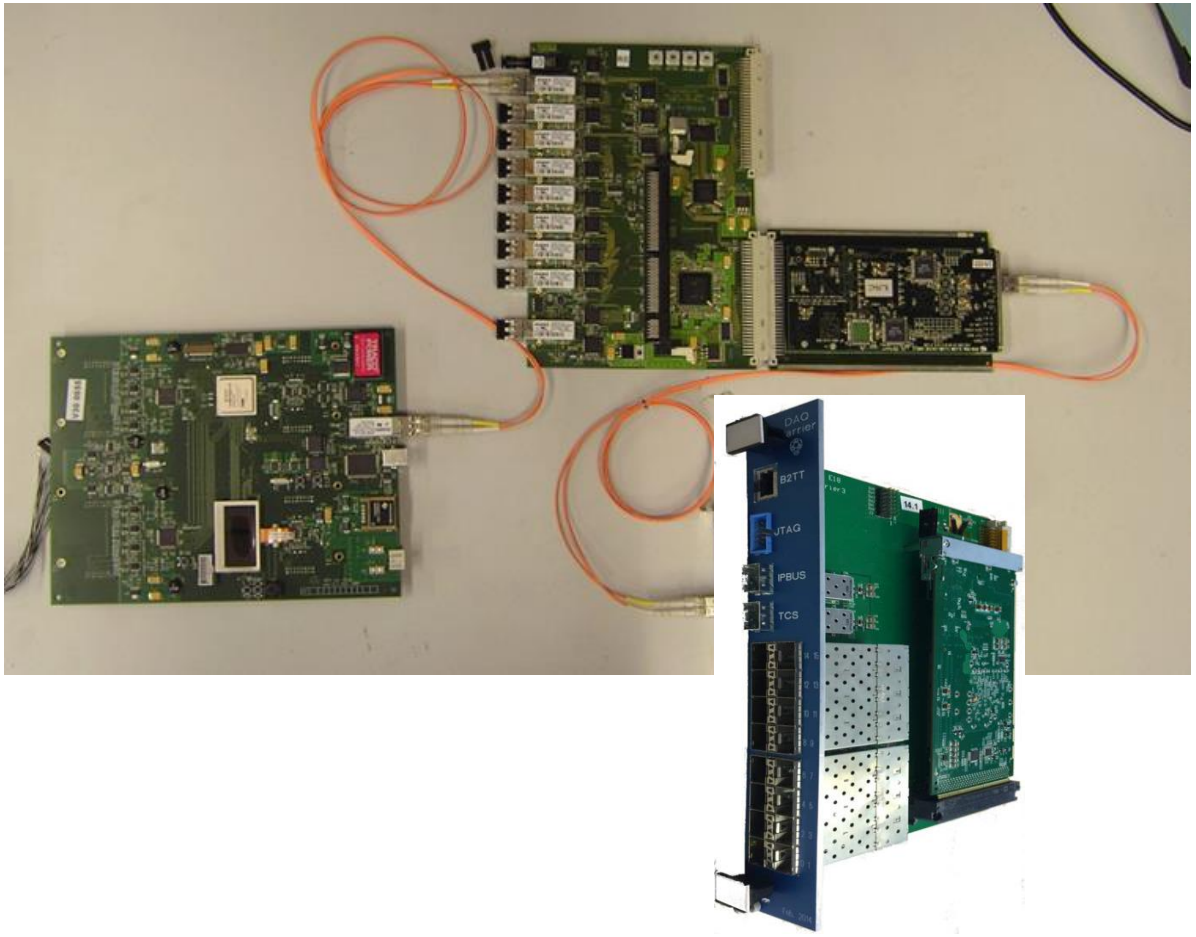
# APV Read Out

Silicon

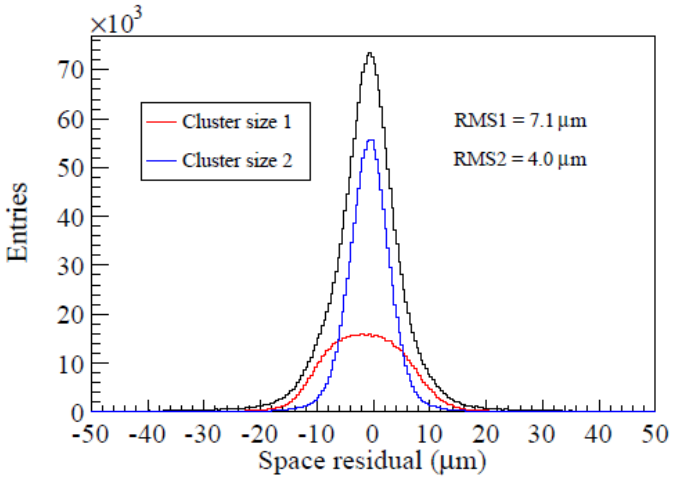


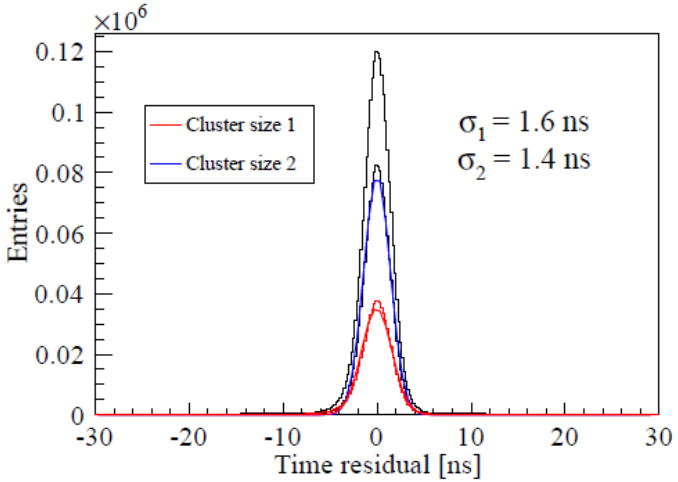

GEM

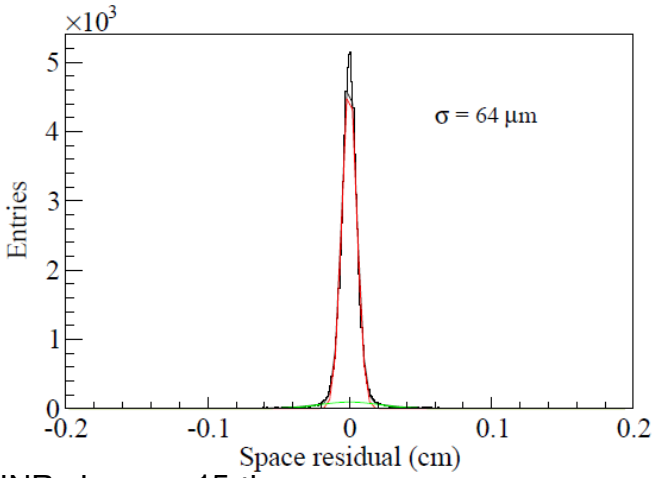


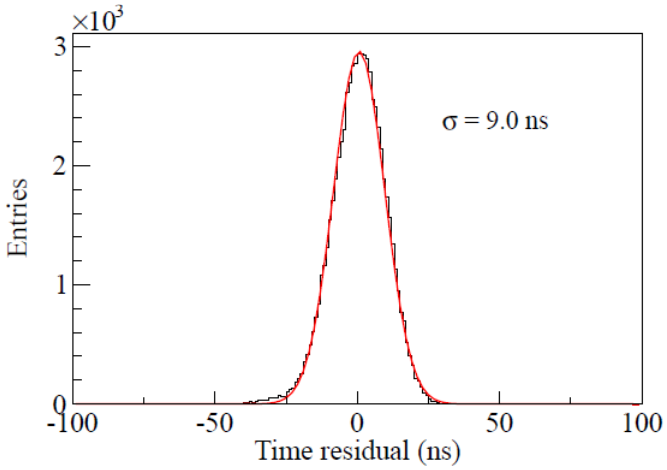



# Silicon and GEM Performance

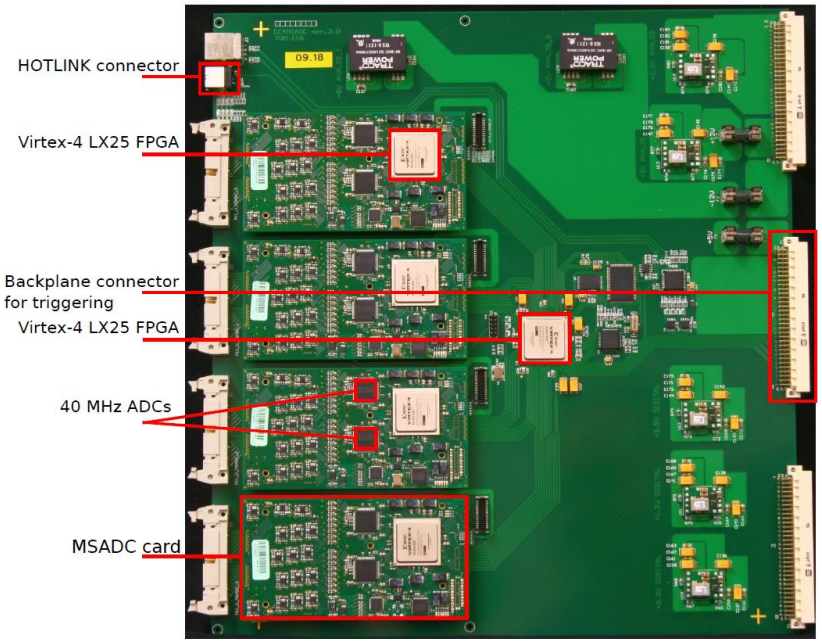


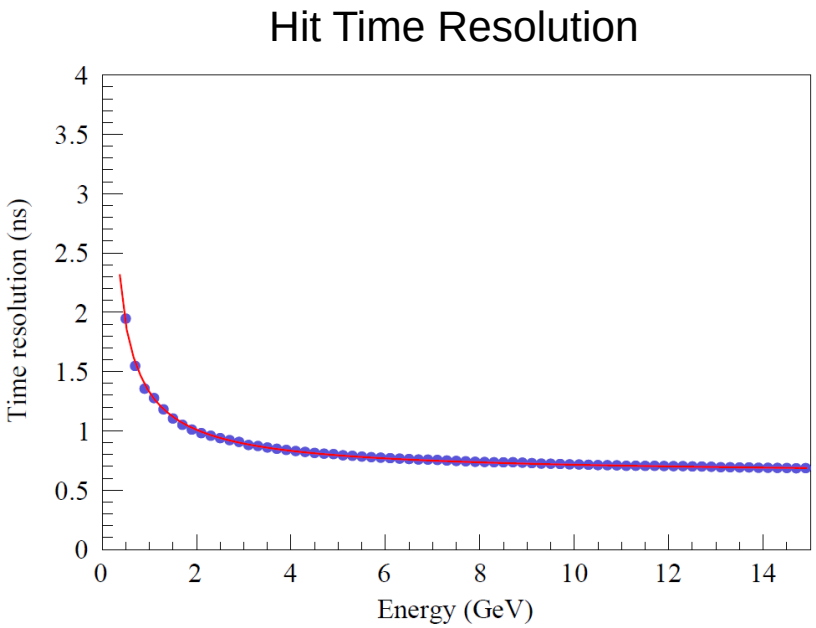



# Sampling ADC




12b@80MHz, 64 channels

Programmable number of samples, tipcle 32

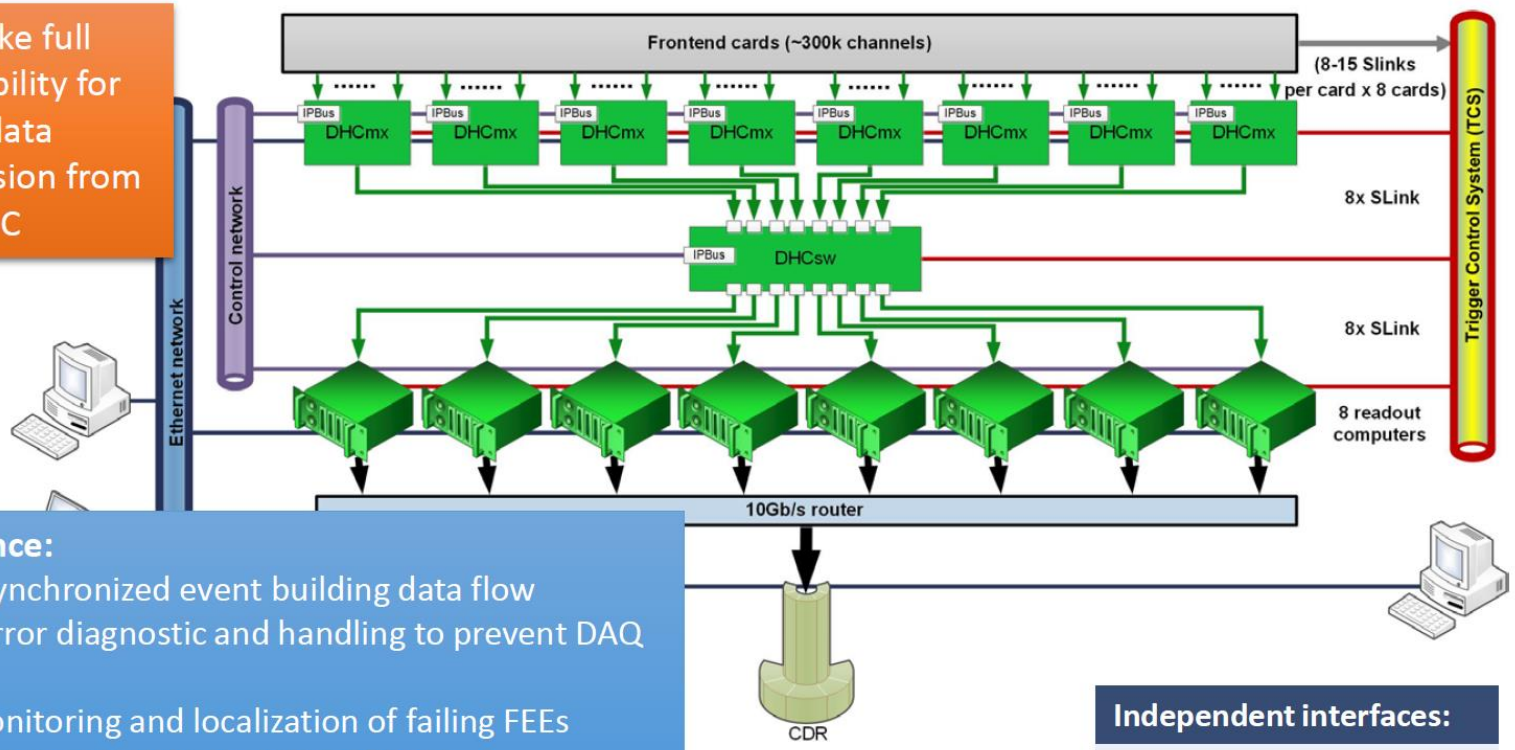
40MB/s limited bandwidth

# iFDAQ

## intelligent FPGA-based DAQ

# iFDAQ Architecture

FPGAs take full responsibility for reliable data transmission from FEEs to PC



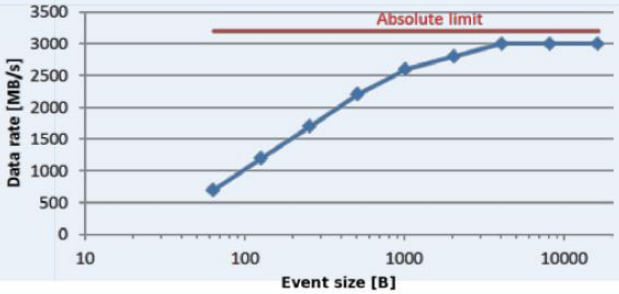

**Intelligence:**

- Self-synchronized event building data flow
- FEE error diagnostic and handling to prevent DAQ crash
  => monitoring and localization of failing FEEs
- Automatic resynchronization of FEEs
  => FEEs can be attached at any time
  => continuous data taking
  => continuous monitoring of data stream and FFE status

**Independent interfaces:**

- synchronization → **TCS (Trigger Control System)**
- data flow (event building) → **SLINK**
- configuration and data flow control -> **Ipbus**

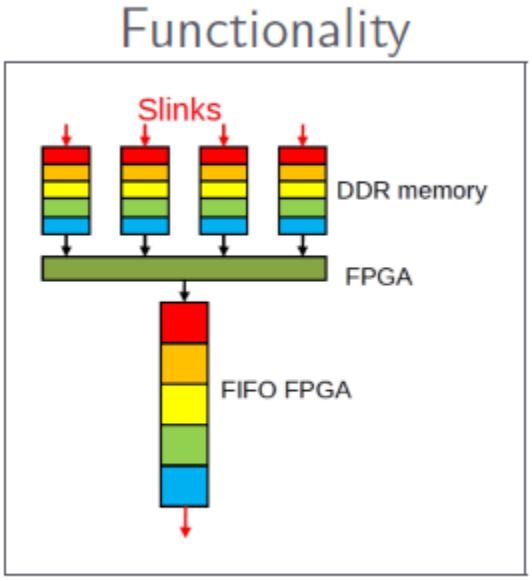
# Data Handling Card

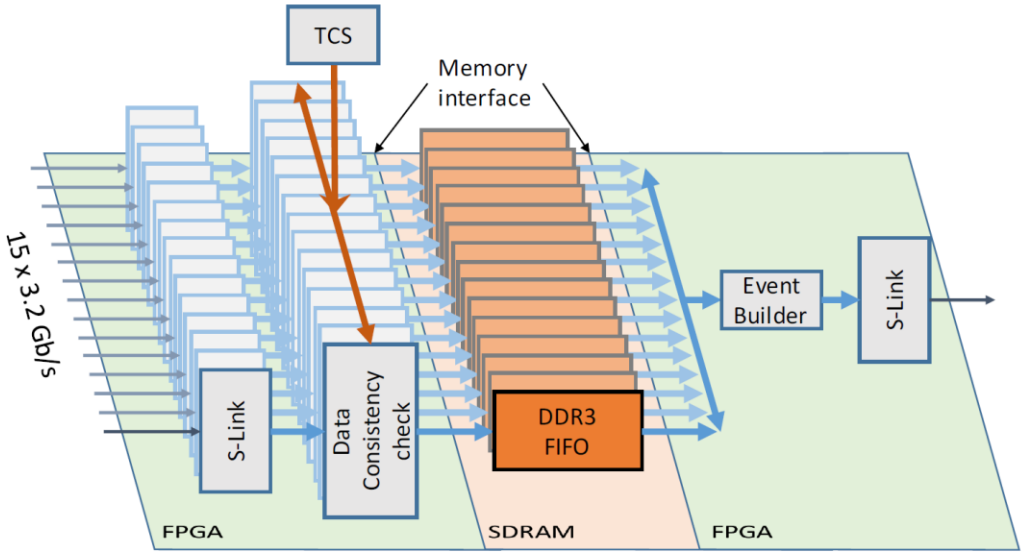
| AMC module | |
|---|---|
| ○ **form factor:** | AMC standard |
| ○ **FPGA:** | Virtex6 XC6VLX130T |
| ○ **memory:** | 4 GB DDR3 SDRAM |
| ○ **firmware:** | • **DHCmx** 12:1 multiplexer [1]<br>• **DHCsw** 8x8-switch |
| ○ **data rate:** |  |



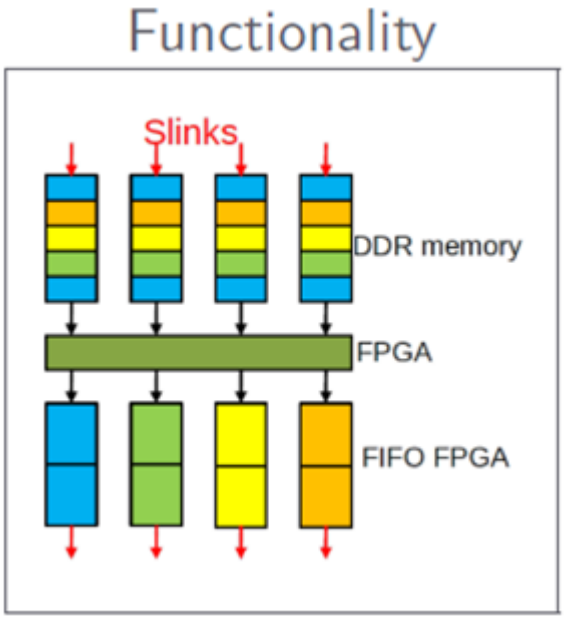
| VME carrier card | |
|---|---|
| ○ **form factor:** | 6 U VME |
| ○ **interfaces:** | • TCS (Trigger Control System) receiver<br>• 1 Gb Ethernet for control network (IPbus)<br>• 16 serial data links (SLINK)<br>• JTAG for backup programming of FLASH |

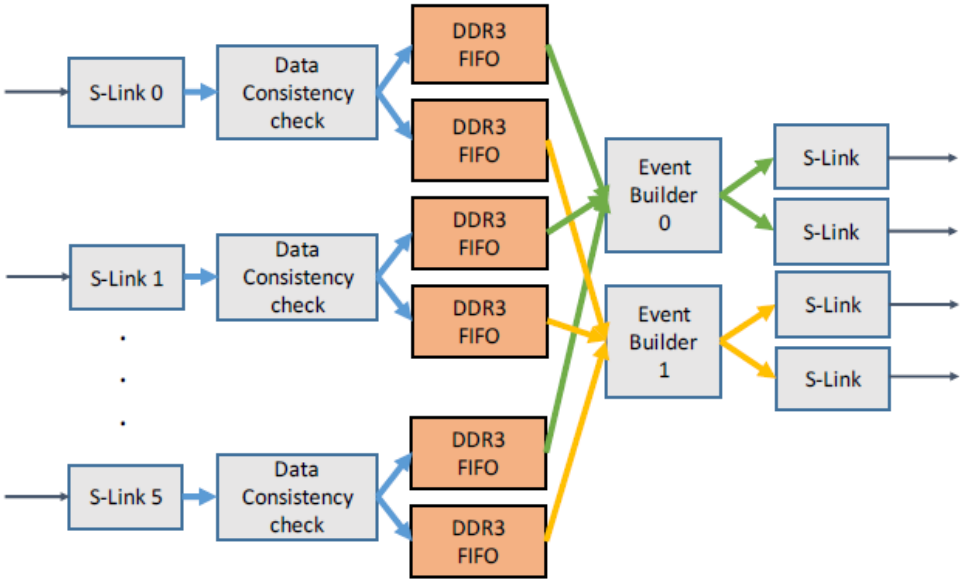
# DHCmx Firmware



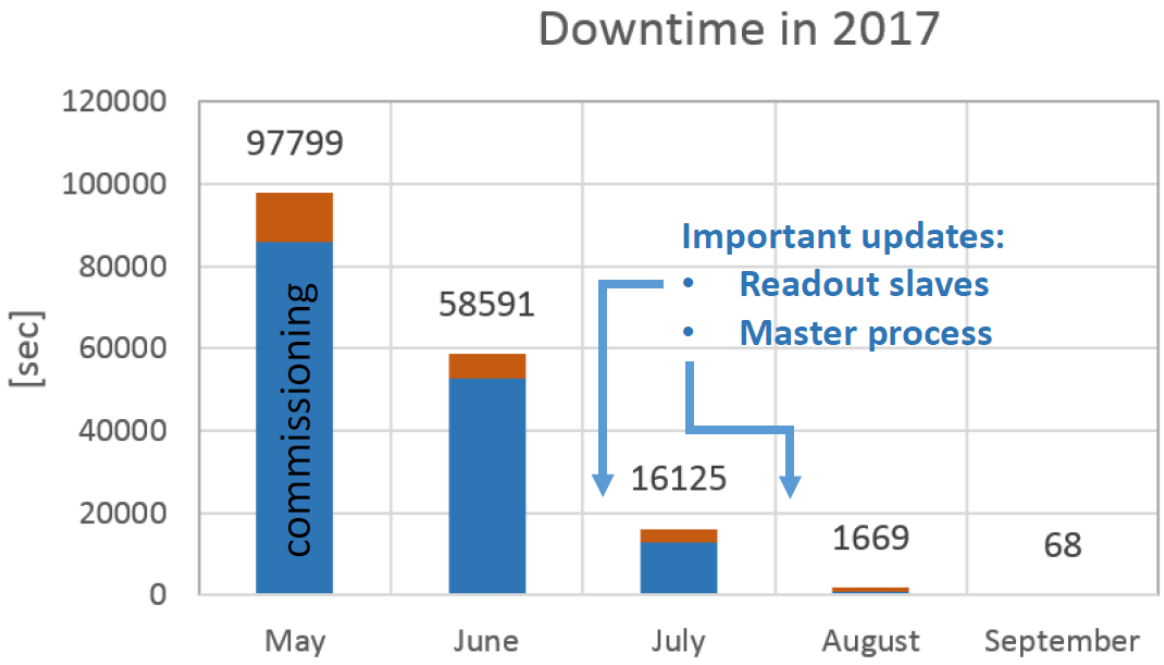
# DHCsw Firmware



# iFDAQ

Hardware Event Builder




PCI/DMA error

Error occurrence usually after scrambled data

Automatic safe stop

Automatic safe stop of data run

- When desynchronization of data flow in event builder
- Data error on switch level in 3 consecutive spills

| UPTIME (%) | 96.35% | 97.74% | 99.40% | 99.94% | 99.99% |
|---|---|---|---|---|---|

Highly reliable

**Two effects:**

1. More stable detectors
2. Upgrades of RCCAR software

# New Developments

# Limits of Current System

**F1 TDC Limitations**

- Trigger latency - 2us
- Trigger rate 40-50kHz
- No further improvements possible

Plan : partial or complete substitute of F1

**APV25 : Silicon, Gem, PGEM, PMM, RICH**

- Trigger latency 4 us
- Trigger rate 40kHz by interface bandwidth, absolute maximum 90kHz

Plan : upgrade to 90kHz or development of trigger less readout

# Limits of Current System : SADC and MSADC

**HCAL1, HCAL2, ECAL1 – SADC 10bit 80MSPS**

- Highly inefficient zero suppression algorithm
- One channel provides 32 samples or 44 bytes of data
- Trigger latency 5us
- 100 kHz @10% occupancy

**ECAL0, ECAL2 – MSADC 12bit 80MSPS**

- One channel provides 32 samples or 68 bytes of data
- Trigger latency 5 us
- Maximum trigger rate limited by interface bandwidth of 20MB/s/64 channels
- 45 kHz @10% occupancy

Plan :

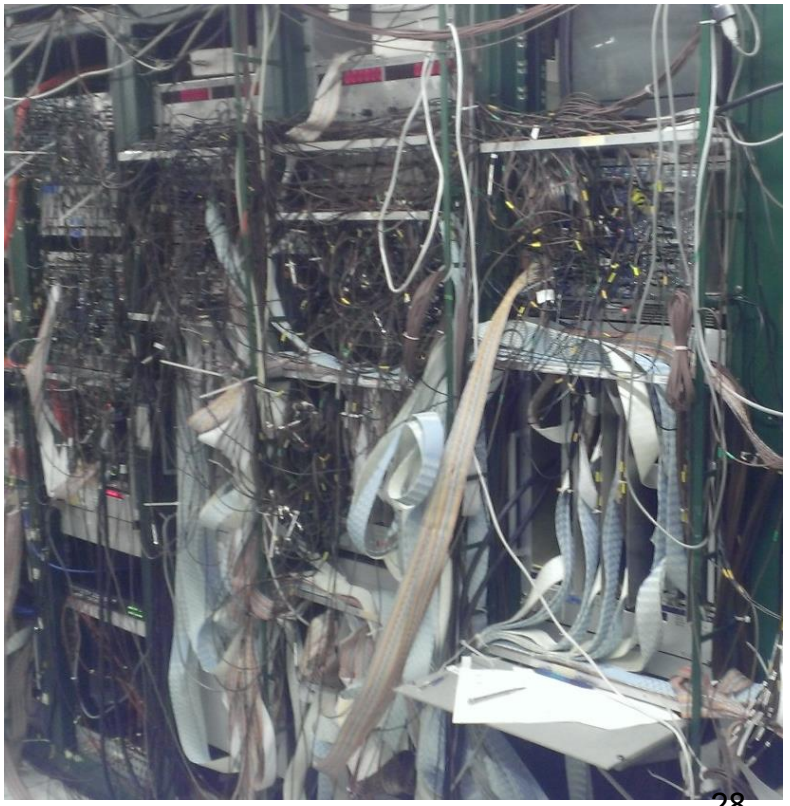
- Implement feature extraction algorithm and transmit Amplitude and Time => 4 Bytes/channel
- Develop new carrier card to convert MSADC to trigger less capable

# Trigger Logic

NIM logical modules
Programmable, analogue coincidence matrixe for target pointing trigger
Very simple trigger functions
Limited programmable features
Limited debugging capabilities

Plan :

- Employ FPGA based trigger processor



# New Developments

**UCF (Unified Communication Framework)**

- Universal protocol for all types of communications between FPGAs
- Single link for trigger, slow control(IPBUS) and data
- Supports different topologies : point-to-point and start like

**FPGA TDC - iFTDC**

**Digital Trigger Processor**

- Process TDC information instead of analogue information
- Provision of AND, OR , VETO processor units
- Build entire trigger logic out of these units within FPGA

**Feature extraction algorithm for calorimeters**

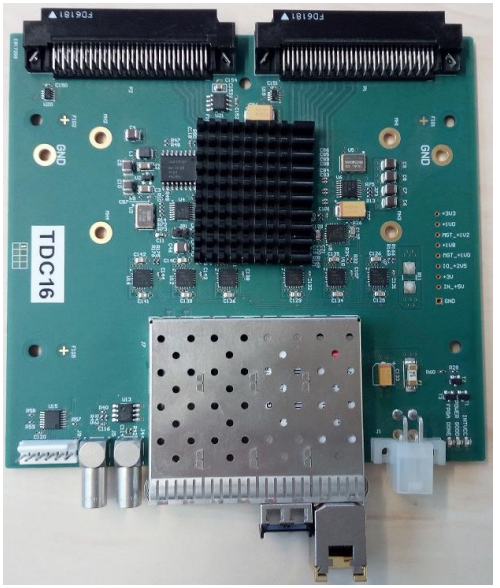
- Develop FIR filter to extract TIME and AMPLITUDE down to SNR = 4

**Develop trigger less FEEs and DAQ for future COMPASS like experiment**

# iFTDC

Features

- ARTIX7 FPGA
- 64 TDC channels
- Bin size : 1 ns, 0.6 ns, 0.3 ns (32 channels)
- Time resolution : 300ps, 200 ps, 100 ps
- PCB exists for MWPC, DC00-DC04
- TDC price ~5 Euro/channel
- It's planned to use the module for CEDAR in 2018
- **Unified interfaces**
  - UCF to TDC MUX 2.5 Gbps , triggered data
  - UCF to Trigger processor , trigger less data




**Requirements for new FEE** :

- two high speed serial links
- UCF protocol for integration to DAQ
- TUM will provide UCF ip cores

# Flexibility of COMPASS DAQ

In order to use COMPASS DAQ one has to comply to the following interfaces :

**Slow Control :**

- Ethernet udp based protocol

**Time distribution system (TCS) :**

- Time precision 40ps, further improvements shall be implemented in FEE
- Accepts NIM inputs, will be compatible with FPGA Trigger Processor

**FEE-DAQ interface: UCF interface**

**DAQ Capability :**

- 10 GB/s sustained
- Triggered and Trigger less data flow

THANK YOU